A Bibliography of Publications on the Intel IA-64 Architecture

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Title word cross-reference

$(10^{31} - 1)/9$ [Hig86]. **$1-Million** [GC97]. ^{TM} [AMD99]. N [Rob05].

-Bit [Rob05].

00 [ACM00].

1.5 [SR03]. **1000** [SSN+01]. **11i** [TOML04]. **12th** [CF00]. **13th** [AH00]. **14th** [KK99]. **16-Way** [Ano01t, AK00]. **16kB** [BMS02]. **16way** [KI01, MSN+01, NTN+01, SYA+01, SUK+01, UMT+01]. **17th** [IEE05]. **1998** [DeG98, JR98]. **1UAXe** [Ano00m].

2 [Ano02b, BH04, CL03, DBC+05, LMOT02, MS03, McN06b, RMC04, SzUK+04, Tho03, WCW+04a, WCW+04b, WCW+04c]. **2.2** [Pra98]. **2000** [Hug00a]. **2001** [Ano00g, CMM01]. **2004** [ACM04a]. **2005** [MHTH07]. **256KB** [RG02]. **25th** [DeG98]. **2nd** [RG02].

32 [Ano04, BDE+04]. **3300-Itanium-Prozessoren** [Ano01f]. **37th** [IEE04]. **390** [GEAS00]. **3D** [Wal02]. **3G** [BBS+01]. **3MB** [WWC02]. **3rd** [ACM06, WWC02].

4way [USK+01].

512 [Fis83, Fis98]. **5L** [IBM00]. **5th** [Ano03].

6-Issue [FO02]. **64** [AAC+04, Ano97,

Ano98a, Ano98b, Ano99c, Ano00b, Ano00e, Ano00d, Ano00i, Ano00j, Ano00n, Ano00p, BCC+00, CFLZ99, Chr96, CHN99, De 06, DBWA00, Die99, Don06, Dos99, Dov99, Dul98, DKK+99, Fan99, FCLZ99, Gig06, Gru00, Gwe97, Gwe99b, Gwe99a, Gwe00a, Hew00a, Hew00b, Haa97, Hal98, HKST99, Har00, HKN+00, HP03b, HP06, HMR+00, HMSW01, IBM00, IKN03, Int99, Int00a, Int00b, Int00e, Int00f, Int00g, Int00h, Int00c, Int00d, Jar99, Jar01, KW01, Kni99a, Kni99b, Kre01b, KKL+00, Mar00, ME02, RT00, RS00, SCV01a, SCV01b, SSN+01, SR00, Son98, ST99, TBGOD99, TRD+00, Tho98, UFG+99, WWCW00, WfL00, ZRMH00a, ZRMh00b, ZRMH00c, ZRMH00d, ZT00].

64-Bit [AMD01, Ano00n, Ano01g, Ano01y, Cha06, AMD99, Ano99e, Ano00f, Ano00g, Ano00h, Ano01a, Ano01z, ET03, Gok96, Pop02].

64-Bit-Architektur [Ano00g].

64-Bit-CPUs [Ano01n].

64-Bit-Welt [Ano01i].

64-Way [Ano00b, Ano00p].

64b [BMS02, NH02].

64bit [Ano01b].

64^{TM} [AMD00, AMD01].

6M [RMC04].

70-443 [MHTH07].

733MHz [Kre01b].

800MHz [Kre01b].

82460GX [DGMM00].

'99 [ACM99].

abstract [VDBN98].

Abstraction [Int00c].

accelerate [EMM00].

Access [BMS02, BC04, CDK00].

Accurate [DH98, SmWHA00, GDN00].

Achieving [SRM+00].

ACM [ACM04a, ACM99].

Acquires [GC97].

Activities [Ave06, Hun06].

Adaptive [Chu06c, YP98].

Add [Kre01a, Rob05].

Address [LCHY03, QD98].

Adds [Ano00m].

Adelaide [KK99].

administration [Pon05].

Adopts [Ano01s].

Advanced [KKL+00, LCHY03, Boh98, NIS00].

Advantage [Geo06].

Advantages [Cha06, Dov99, Int00a].

AES [WWCW00].

Again [Ano01d].

AIX [Ano98b, IBM00].

ALAT [LCHY03].

Algorithms [CHI+03, Har00, Int00i, Int03a, Int03b, ST99, Har03].

allein [Ano01i].

Allianz [Ano01e].

allocation [RDG08].

Alpha [Ano00l, Ano01x, Kar07].

Alpha-Architektur [Ano01x].

AlphaServer [Ano02a].

alter [Anoxx].

Alternative [Ano01c, Liu06, YP98].

Am [Ano01n].

Amazing [GC97].

AMD [AMD01, Ano01y].

Analysis [Cam03, BBS+01, Gep00, SmWHA00, Sve02].

Analyzer [Ano01y, DBC+05].

anatomy [GO98].

Anbieter [Ano01x].

angepasst [Ano01i].

Annual [USE02].

ante [Ano01n].

Anwendungen [Ano00i].

AOL [Ano01v, GC97].

API [Ano00l].

Aplio [Ano00m].

Application [Fis79, Int99, Int00e, Int00d, WYX+08].

Applications [Ano02d, BBC+02, FURM00a, FURM00b, IBM00, JM02, KKH+01, Sto02, TBB01, BDE+04].

Applied [SDC01].

Applikationen [Ano01i].

Approach [HP03a, HPAD+06, EMM00, FFY05].

approaches [Ano99c].

Approaching [Ser02].

apps [Ano00k, Ano01r].

April [ACM00, KK99, NIS00].

architectural [mWH98].

Architecture [AMD99, AMD01, AAC+04, Ano99e, Ano02a, ACM+04b, BBC+02, CFLZ99, Cla06, CHI+03, DeG98, Dos99, Dul98, FCLZ99, Gru00, Hew00a, Hew00b, HKST99, HP03a, HP03b, HPAD+06, HMR+00, Int99, Int00e, Int00f, Int00g, Int00h, Int00d, Int03a, Int03b, Jar99, Kni99a, KFL99, KKL+00, Li01, Mär03b, McN06a, Moo06, SR98, SYA+01, SCHL03, SLHC04, TBGOD99, TBB01, UFG+99, Wir99, WfL00, ZRMh00b, ZRMH00c, ZRMH00d, Ano00g, Ano02c, ACM+98, BGM+00, BC04, CDK00, ET03, FFY05, GEAS00, HDL+07, IKN03, Sco01,

Tri00, ZRMH00a, Dor99]. **Architectures** [Cam03, Fis83, HKN+00, SMJ99, TLS90, Fis98, SJS00]. **Architektur** [Ano00g, Ano01e, Ano01x, Ano01m]. **Area** [CMM01]. **Arena** [Ano01q]. **Aren't** [VL97]. **ARITH** [IEE05]. **ARITH-17** [IEE05]. **Arithmetic** [CHN99, IEE05, KK99, TOML04, Ano02c, LMOT01, LMOT02, dDDL04]. **Arms** [Gea06]. **arrived** [Ano01a, Ano01b]. **Article** [Ano01p]. **assembler** [DBC+05]. **Assembly** [TBGOD99, AMR00]. **Assistance** [Int00k]. **Association** [Ano00m]. **AT75C310** [Ano00m]. **Athlon** [Ano99a]. **Atlanta** [ACM99]. **attracts** [Ano00k, Ano01r]. **Attributes** [Cam03]. **Auch** [Ano01i]. **Aufgabe** [Ano01x]. **August** [AH00, CF00, IEE97, IEE99, IEE00]. **Australia** [KK99]. **Automatic** [AGMM00, NTN+01, ZWG+97]. **Availability** [Qua00a, Qua00b]. **Avenue** [Ano00m]. **AVP** [Ano00l]. **Awards** [Kro00a]. **aware** [GDN00]. **AzusA** [Ano01t, AK00, KI01].

Back [GC97]. **Backend** [Liu06]. **Backup** [Ano00l]. **backward** [Ano01y]. **Bandwidth** [Die99, RG02]. **Barcelona** [DeG98]. **BART** [CMM01]. **Based** [Ano00n, BBS+01, Int00j, TOML04, WWC02, Ano00e, Ano06, BDE+04, BGM+00, BMM99, BM00, CHT02, JM02, KW01, Kob01, Pon05, TBB01, WCW+04a, WCW+04b, WCW+04c]. **Basic** [Fis79, Kre01a, McN06a]. **Basics** [Kni99a]. **Basics/Introduction** [Kni99a]. **Basis** [Ano99b, Ano00e, Ano01f]. **Bay** [CMM01]. **be** [Ano98b, Ano00h]. **Bea** [Ano01c]. **Beam** [BBS+01, Pin06]. **Beats** [Ano00h]. **Behind** [Col05]. **Benchmark** [Ano01d]. **Best** [Ano00m]. **Betriebssysteme** [Ano01i]. **better** [Ano01y]. **Beyond** [Fis79, Tho98]. **bieten** [Ano01c]. **big** [Ano00a, BBS+01]. **Billion** [Ser02]. **Binary** [CHN99, GEAS00, Lew99, SmWHA00]. **Bingaman** [BBS+01]. **Bioinformatics** [Anw06]. **Biological** [KA06]. **Biopolis** [Ano06]. **Bit** [AMD01, Ano00g, Ano00n, Ano01g, Ano01i, Ano01n, Ano01y, Cha06, Rob05, Wal02, AMD99, Ano99e, Ano00f, Ano00h, Ano01a, Ano01z, ET03, Gok96, Pop02, Sco01, Wal02]. **bleiben** [Ano01q]. **BLISS** [Bre02]. **Blocks** [Ano00m, Ano01s, Fis79]. **boolean** [VB01]. **Boost** [Ano00f]. **boosts** [Ano01v]. **booting** [Dor99]. **bottlenecks** [CDK00]. **bow** [Haa97]. **Box** [Ano00l]. **Branch** [SMJ99, DH98, HSS99, YP98]. **breaking** [CH03]. **breite** [Ano01e]. **Bridge** [Ano00l]. **Bridging** [ACM04a, VDBN98]. **Briefs** [GC97, Leh00a, Leh00b]. **Bright** [Ano02a]. **Bus** [SDC01]. **Business** [GC97, Anoxx]. **buyers** [Ano98a]. **Bypassed** [FO02]. **Bytes** [CMM01].

C [Ano02d, IBM00, Kul06, dD00b, dD00a]. **CA** [IEE03, ACM00, CF00, IEE02, Ano01s]. **Cache** [BMS02, BH04, Int00a, RG02, RMC04, WWC02, BC04, CL03]. **cached** [LC99]. **Caches** [VL97]. **California** [IEE97, IEE99, IEE00, USE00, USE02]. **Call** [Gea06, Ano01k]. **Canada** [Ano00l]. **Candidate** [NIS00]. **Cape** [IEE05]. **Carlo** [SCL06]. **Cartridge** [Sam00, SCV01a, SCV01b]. **Case** [Kul06]. **CD** [Ano00l]. **Celebrates** [Ano01d]. **cell** [WSO+06]. **Cellulars** [BBS+01]. **Center** [Ano01d, Sha03]. **Centric** [BH04]. **CEO** [Ano01v]. **CERN** [Pin06]. **CGO** [IEE03]. **Challenge** [Kre01a]. **Challenges** [Cha06, Li01, Ser02, Smi00, Wir99, SK01]. **Chancen** [Ano00j, Ano00d]. **chances** [Ano00d]. **Changes** [BBS+01, Ano00j]. **characterization** [HDL+07]. **Chassis** [Ano00l]. **Cheney** [BBS+01]. **Chip** [Ano01i, DGMM00, GC97, Pau01, Ano98b, Ano00a, Ano01v, BGM+00, WWC02]. **Chipmaker** [Ano01y, Anoxx]. **Chips**

[Col05, IEE97, IEE99, IEE00, Ano00e, Ano00f, Pop02, Ano99b, Ano00e]. **Choice** [Kro00a]. **Choices** [Ano00k, Ano01r]. **Chronicles** [Col05]. **Circuits** [HKLS00, IEE02, Moo65, CBF01, Gep00]. **Clix** [CMM01]. **Clock** [AWB02, DTZR00, RT00, TRD+00, WAB02, BM00]. **ClustalW** [Chu06c]. **Cluster** [Ano99b, Wol04, Ano00e, Ano00e]. **Clusters** [Joh06b]. **CLX** [CMM01]. **CO** [ACM01]. **Cod** [IEE05]. **Code** [AMR00, Ano01s, BCC+00, IEE03, Kul06, LC99, VBLvdG08, WWK+01]. **Codes** [Roo06]. **Collection** [HMSW01, SDC01]. **COM** [Ano00m]. **COMAs** [QD98]. **comes** [Ano00g]. **Coming** [Wol04]. **communities** [ACM04a]. **Compact** [SDC01]. **Company** [GC97]. **Compaq** [Ano01q, Ano01x, Ano00a, Ano00o, Ano01w]. **Comparative** [Cam03, HDL+07]. **Compare** [Ano01d]. **compatibility** [Ano01y]. **compilation** [GDN00]. **Compiler** [Ano01i, BCC+00, BCD+92, DKK+99, DSR01, Fan99, Gwe99c, HKS+04, Hua06, LC99, Roo06, SLHC04, ZRMh00b, ZRMH00c, ZRMH00d, CDK00, IKN03, ZRMH00a]. **Compiler-driven** [LC99]. **Compilers** [Ano02d, KFL99, Moo06, CF00, FFY05]. **Compiling** [Hua06, Li01]. **Complex** [Lew99]. **Complexity** [SRM+00]. **Components** [Moo65]. **Comprehensive** [WfL00]. **compression** [LC99, Luc00]. **CompuServe** [GC97]. **Computable** [BM05]. **Computation** [HKST99]. **computations** [EMM00]. **Computer** [Ano00m, DeG98, HP03a, HPAD+06, IEE05, KK99, Mär03b]. **Computers** [Ano03]. **Computing** [ACM01, ACM04a, ACM06, Ano00m, Ano01e, Ano01g, BBS+01, Gep01, GHH+01, KBC+97, KvG01, Mar05, Pin06, SC00, Tak06, Tan06, Anoxx, CH03, CF00, CHT02, FFY05, GHH+02, GO98, SCV01b, WSO+06]. **Conference** [ACM99, ACM04a, AH00, Ano03, Ano06, IEE02, NIS00, USE02, ACM06, Pop02]. **Confronts** [Die99]. **Confusion** [GC97]. **Connect** [Ano00l]. **consider** [SCV01b]. **Considerations** [ZRMh00b, ZRMH00c, ZRMH00d, ZRMH00a]. **constraints** [EFKR01]. **Control** [CMM01, SMJ99]. **Controlled** [SLHC04]. **Convergence** [GC97, GEAS00]. **coprocessors** [CS00]. **Core** [AWB02, MP01, MB05, McN06b, Sha00a, Sha00b, WAB02]. **Corp** [Ano00m]. **Corporation** [Ano00l, Ano00m, Ano00l]. **correct** [dDDL04]. **correlating** [HSS99]. **cost** [Anoxx, Ano01y, Sib98a]. **cost-efficient** [Sib98a]. **could** [Anoxx]. **counted** [Kro00a]. **Counter** [Geo06]. **Courseware** [BBS+01]. **CPR** [SMJ99]. **CPU** [Ano00b, Ano00p, Ano01y, Ano01z]. **CPU2000** [HDL+07]. **CPU2006** [HDL+07]. **CPUs** [Ano01n, Ano00c, Ano00c]. **Cramming** [Moo65]. **creature** [Ano01v]. **Criteria** [Roo06]. **Critic** [Lew99]. **Crystals** [BBS+01]. **current** [CDK00]. **custom** [AMR00]. **customizable** [FBF+00]. **Cycle** [BMS02]. **Cycles** [HMSW01].

Data [AMD99, BC04, BH04, Sha03, VL97, BMM99, CDK00, DKM01, EMM00, HSS99]. **Database** [Anw06, Gok96, MHTH07]. **Databases** [Ano00j, MLH+00]. **Datapath** [FO02]. **Datenbanken** [Ano00j]. **day** [Haa97]. **Deals** [Ano98a]. **Death** [Tuo02]. **Debug** [JPG02]. **Debut** [Ano01m]. **December** [IEE04]. **Decision** [Cla06, SmWHA00]. **Decryption** [Int00i]. **Defense** [BBS+01]. **Defining** [War97]. **delay** [EFKR01]. **demonstrates** [Ano00e]. **demonstriert** [Ano99b, Ano00e]. **demos** [Ano00f]. **Demystifying** [Son98]. **Denver** [ACM01]. **Departments** [Ano99a, Ano01d]. **Deshalb** [Ano01x]. **Design** [ACM99, ACM00, CBF01, DTZR00, EM00, Gok96, Gwe99c, Roo06, Ser02, ZRMh00b, ZRMH00c, ZRMH00d, LLC99, ME02, SR00,

SK01, ZRMH00a]. **designed** [BDE+04]. **Designing** [DBWA00, MHTH07]. **Designs** [Ano00m]. **Desktop** [FURM00a, FURM00b]. **Detailed** [Jar99]. **details** [Haa97]. **Developer** [Int99, Int00b, Int00j, Int00e, Int00f, Int00g, Int00h, Pop02]. **Developers** [Int00a, Int00d, Tri00]. **Developing** [Sto02, TBB01]. **Development** [POY+01, UFG+99]. **Devices** [Gep00]. **diagrams** [SmWHA00]. **dictionary** [Luc00]. **Diego** [ACM00, USE00]. **DIG64** [DBWA00]. **dimensional** [SJS00]. **Direct** [MSP98]. **Directed** [Smi00, IEE03]. **Discloses** [AMD99, Gwe99b]. **Disclosures** [Hew00a]. **discounts** [Ano98a]. **Distributed** [Joh06a]. **Distribution** [TRD+00, RT00]. **diverging** [Ano01v]. **Divide** [Int03a]. **Division** [CHI+03, Har00, Int03b, Rob05]. **double** [dDDL04]. **double-extended** [dDDL04]. **DoubleVision** [Ano00l]. **Down** [GC97]. **Drive** [GC97]. **driven** [LC99]. **Drivers** [Chu06b]. **drum** [Ano01k]. **Dual** [MB05, McN06b]. **Dual-Core** [MB05, McN06b]. **Dual-Thread** [MB05]. **DVD** [GC97]. **Dynamic** [Gwe99c, Ram93, BDE+04, BM00, CLS00, QD98, WWK+01]. **Dynamics** [KA06].

earliest [Ano00g]. **EarthLink** [Ano01v]. **Easysoft** [Ano00l]. **ebnen** [Ano01e]. **edition** [Ano00m]. **Editor** [Cra00]. **Effective** [KKN06, VB01]. **Efficient** [CWY+08, SmWHA00, Sib98a]. **Einblick** [Ano01u]. **Einführung** [Mär03b]. **Electronic** [Ano00l, Ano99a]. **Elementary** [Mar00, Mar03a, dDDL04]. **Elements** [Gwe99c]. **ELI** [Fis83, Fis98]. **ELI-512** [Fis83, Fis98]. **Elimination** [WfL00, KKN06]. **Embedded** [FFY05, Leh00a, Leh00b, FBF+00, Haa97, LC99]. **embedding** [LLC99]. **emphasis** [IEE03]. **empirically** [SS03]. **Employs** [Ano00b, Ano00p]. **Encryption** [GC97, NIS00]. **end** [Ano01q]. **Ende** [Ano01m]. **Energy** [BBS+01]. **Engineering** [Ano00m, SDA05]. **Enhanced** [Ano00l]. **Enough** [VL97]. **Enterprise** [Ano00k, Ano01r]. **entschieden** [Ano01x]. **Entwicklung** [Ano01m, Ano01o]. **Environment** [KBC+97, UFG+99, SCV01b, VVP+04]. **Epic** [Ano01e, AMR00, ACM+98, ACM+04b, BC04, ET03, SR98, SMJ99, SC00, SzUK+04, Son98, Mat04, Ano01e]. **Epic-** [Ano01e]. **Erfolg** [Ano00i]. **erfolgreich** [Ano01i]. **erkaufen** [Ano01x]. **erst** [Ano00g]. **Europe** [BBS+01]. **Evaluating** [De 06]. **Exam** [MHTH07]. **Exception** [Int00k, dD00b, dD00a]. **executables** [SDA05]. **Execution** [Ano04, ACM+04b, BDE+04, ZT00, ACM+98, SR00, WWK+01]. **Exits** [TLS90]. **Expensive** [Lew99]. **Experience** [Jur06]. **Experiences** [Joh06b, USE00]. **experimental** [WCW+04a, WCW+04b, WCW+04c]. **Explanation** [Kre01a]. **Explicit** [VDBN98]. **Explicitly** [Ano01e, SC00, Haa97]. **explicitly-parallel** [Haa97]. **Explicitly-Parallel-Instruction-Computing-** [Ano01e]. **Expo** [Ano06, JR98]. **Export** [GC97]. **Express** [Ano01f]. **Express5800** [SSN+01]. **Express5800/1000** [SSN+01]. **Extended** [Ano01d, VDBN98, dDDL04]. **Extensible** [Dor99]. **extension** [KKN06]. **Extensions** [TH99]. **extraction** [GDN00]. **Eyelet** [Ano00m].

Fab [MC07]. **face** [Ano01v]. **factor** [Hig86]. **Factorization** [QOV09]. **Family** [Ano04, Hew01, POY+01]. **fassen** [Ano01q]. **Fast** [Lew99, Mar05, dDDL04, Mar03a]. **Fast-Start** [Mar05]. **FBI** [Ano01v]. **Feature** [SCV01b]. **Features** [Ano00b, Gwe99b, Kni99b, Qua00b]. **February** [IEE02]. **Feedback** [Smi00, IEE03]. **Feedback-Directed** [Smi00, IEE03]. **feiert** [Ano01m]. **Field**

[SzUK+04]. **Field-testing** [SzUK+04]. **File** [FO02]. **Filesystem** [Joh06a]. **FileZerver** [Ano00m]. **Finalists** [WWCW00]. **find** [Ano01v]. **Finding** [Mat04]. **Finds** [BBS+01]. **Finnish** [Ano00m]. **Firms** [GC97]. **Firmware** [Dor99, MSN+01]. **First** [Ano01g, BBS+01, Gep01, Haa97, Kre01b, Pin06, RS00, TRD+00, USE00, RT00, SR00]. **Fisherman** [IEE03]. **FLAME** [VBLvdG08]. **Floating** [CHN99, Int00k, TOML04, Ano02c, LMOT01, LMOT02]. **Floating-Point** [CHN99, TOML04, Int00k, Ano02c, LMOT01, LMOT02]. **Floorplan** [MLH+00]. **Flow** [CWY+08]. **Focuses** [Die99]. **forces** [Ano00c]. **forciert** [Ano00c]. **forecast** [Gep00, Gwe97, Gwe00a]. **Forefront** [Ano00b, Ano01h]. **Formal** [Har00, Har03, VB01]. **formats** [AMR00]. **forthcoming** [Ano00f]. **Fortran** [Hew01, Ano02d]. **Forum** [AMD99, Haa97]. **four** [Sco01]. **fourth** [Ano00g]. **framework** [AMC+03, mWH98]. **France** [Ano03]. **Francisco** [IEE02, IEE03]. **FreeBSD** [Ano00l]. **Freemont** [Ano00m]. **Frequency** [RMC04]. **Frontiers** [ACM06]. **fruhestens** [Ano00g]. **Fullchip** [MLH+00]. **Fully** [FO02]. **Fully-Bypassed** [FO02]. **function** [Mar03a]. **Functions** [AAC+04, BM05, HKST99, HKN+00, Mar00, ST99, Tho03, dDDL04]. **fundamental** [Anoxx]. **Fused** [BM05, Kre01a]. **Fused-mac** [BM05]. **Fuss** [Ano01q, BBS+01]. **Future** [Ano02a, Cam03, MC07, Roe98, SK01, Mat04, Ano01a, Ano01b, Tho98].

Gang [Ano01h]. **Garbage** [HMSW01]. **Gateway** [Ano00m]. **gating** [BM00]. **GCC** [Ave06, Liu06]. **Gcom** [Ano00m]. **Gears** [Nan98]. **Gelato** [Ano06, Gea06]. **GEM** [BCD+92]. **General** [USE02]. **generating** [SS03]. **Generation** [AWB02, Anw06, BMS02, HN01, IEE03, NH02, SR03, TRD+00, WAB02, Dor99, RT00]. **Generator** [BCC+00]. **Georgia** [ACM99]. **German** [Mär03b, Ano00c, Ano00e, Ano00d, Ano00g, Ano00i, Ano00j]. **Get** [Hug00b, Ano98a]. **Gets** [Ano00f]. **GHz** [SR03]. **GNUPro** [Ano00m]. **good** [Ano00d]. **GPT** [Chu06a]. **Grace** [GC97]. **Grid** [BBS+01, Lee06, Hun06, Pin06, Tak06, Wol04]. **Grids** [Joh06b]. **Growth** [GC97]. **Guest** [Cra00]. **GUI** [Ano00m]. **Guide** [Ano04, Eng00, Int99, Int00b, Int00h]. **Guidelines** [DBWA00]. **gute** [Ano00d].

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Dor99, DKK+99, Eng00, GC97, Gru00, Gwe97, Gwe99b, Gwe00a, Gwe00b, Haa97, HP03b, HP06, Hua06, Kre01b, McN06a, McN06b, Moo06, Pau01, Pop02, SCHL03, SLHC04, Sha99, Sha00a, Sve02, Tho98]. **Intel-Plattform** [Ano01c]. **Intel-Server** [Ano00j]. **Intel/H** [Haa97]. **Intel/H-P** [Haa97]. **Intel(R)** [DSR01, SDC01]. **Intels** [Ano99b, Ano00c, Ano00e, Ano00d, Ano00g]. **Interactive** [FURM00a, FURM00b]. **interest** [Ano00k, Ano01k, Ano01r]. **Interface** [Era06, Int00b, Dor99]. **International** [ACM00, AH00, CF00, DeG98, IEE02, IEE03, IEE04]. **Internet** [GC97, TH99]. **Interoperability** [DBWA00]. **Interval** [KvG01]. **introduced** [Ano99a]. **Introduces** [Ano01d]. **Introducing** [Cra00, HMR+00]. **Introduction** [Cra00, Kni99a, Mär03b]. **Inverse** [Mar05]. **Investigations** [She06]. **Ion** [BBS+01]. **ISA** [Die99]. **Ischia** [ACM06]. **ISP** [Ave06]. **ISPD** [ACM00]. **ISPD-00** [ACM00]. **ISSCC** [IEE02]. **Issue** [FO02, Kob01, Ano99e, mWH98, RF93]. **issues** [GEAS00]. **Italy** [ACM06]. **Itanium** [Ano00b, Ano00c, Ano00p, Ano01c, Ano01f, Ano01e, Ano01i, Ano01q, Ano01u, Ano01x, Ano02b, Ano06, BH04, CL03, McN06b, Wal02, Ano99a, Ano99b, Ano99d, Anoxx, Ano00a, Ano00c, Ano00e, Ano00f, Ano00g, Ano00h, Ano00k, Ano00n, Ano00o, Ano01a, Ano01d, Ano01g, Ano01h, Ano01n, Ano01k, Ano01m, Ano01o, Ano01j, Ano01l, Ano01p, Ano01r, Ano01t, Ano01s, Ano01w, Ano01y, Ano01b, Ano01z, Ano02a, Ano02c, Ano04, AK00, Ave06, BDE+04, BBC+02, BBS+01, BMS02, Cam03, CH03, Cha06, Cla06, CHT02, CHI+03, Cra00, DTZR00, DBC+05, Int00n, DSR01, Eng00, ET03, FO02, Geo06, Gep01, Gwe00a, Gwe00b, Hew01, HP03b, HP06, HKS+04, Int00j, Int00h, Int00i, Int00k, Int00l, Int00m, Int03a, Int03b, JM02, Joh06b, Jur06, KKH+01, KNH+01, Kob01, KI01]. **Itanium** [Kre01a, Kre01b, Kul06, Lau06, Li01, LMOT01, LMOT02, Liu06, Mar03a, MLH+00, MS03, MB05, McN06a, MSN+01, Moo06, NTN+01, POY+01, Pau01, Pon05, Pop02, Qua00a, Qua00b, RG02, Roo06, RMC04, Sam00, SCV01a, SCV01b, Sco01, SYA+01, SCHL03, SLHC04, Sha03, Sha99, Sha00a, Sha00b, SA00, SUK+01, SzUK+04, SDA05, SR03, Sve02, Tho03, TOML04, Tri00, TBB01, Tsu01, USK+01, UMT+01, WCW+04a, WCW+04b, WCW+04c, WWC02, WAB02]. **Itanium-2** [LMOT02, WCW+04a, WCW+04b, WCW+04c]. **Itanium-based** [Ano06, Int00j, TOML04, BDE+04, CHT02, JM02, Kob01, Pon05, TBB01]. **Itanium-Chips** [Ano99b, Ano00e]. **Itanium-Entwicklung** [Ano01o]. **Itanium(R)** [GHH+02, HDL+07]. **Itanium**^{TM} [AWB02, GHH+01, HN01, NH02, SDC01]. **iWarp** [GO98]. **IX** [IEE97].

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[FURM00a, FURM00b, MB05]. **Threading** [McN06b, VDBN98]. **threads** [WCW+04a, WCW+04b, WCW+04c]. **Threads.h** [Ano00l]. **Time** [IKN03]. **Timing** [MLH+00, GDN00]. **Tip** [Ano01u]. **Today** [Tan06]. **Together** [HP03b]. **Tomorrow** [Tan06]. **Toolkit** [Ano00m]. **Tools** [Ano00m, Cha06, TBGOD99, Wol04, FFY05]. **Tools.h** [Ano00l]. **Top** [Anoxx, Ano00b, Ano00p]. **topology** [Sib98a]. **TPHOLs** [AH00]. **Track** [USE02]. **Tracking** [CWY+08, She06]. **Trade** [MSP98]. **Trade-Offs** [MSP98]. **training** [MHTH07, YP98]. **Transaction** [HKS+04]. **Transcendental** [HKST99, ST99]. **transfer** [CDK00]. **transformations** [AGMM00]. **Transforming** [YAK00]. **Transistor** [Ser02]. **Transit** [CMM01]. **translation** [GEAS00, QD98]. **translator** [BDE+04]. **Transparent** [ZT00]. **Transport** [AMD99]. **Trends** [CMM01, Boh98]. **Tridia** [Ano00l]. **Trillian** [Ano00h]. **Triumphs** [Li01]. **TurboLinux** [Ano00f]. **TurnSafe** [Ano00m]. **Tutorial** [Int00d, Jar99, KFL99]. **two** [BDE+04, SJS00, YP98]. **two-dimensional** [SJS00]. **two-level** [YP98]. **two-phase** [BDE+04].

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[Wal02, Ano00h, Ano00n, Ano01z, Ano02d, KKH+01]. **wird** [Ano01x]. **within** [LLC99]. **Wolfram** [Ano00m]. **Wonderful** [Pra98]. **Word** [Fis83, Fis98]. **Work** [Dul98, Gwe99c, Haa97]. **work-a-day** [Haa97]. **worker** [Ano01v]. **Workloads** [HKS+04]. **workqueuing** [VBLvdG08]. **Workshop** [CF00, USE00]. **Workstation** [Ano00l, DGMM00, Kob01, Kro99, Ano01j]. **Workstations** [Pau01]. **World** [Cam03, Pra98].

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York [NIS00]. **Yosemite** [Ano00l].

zum [Ano01x]. **zur** [Ano01x]. **zwei** [Ano01m].

References

Akutin:2004:HOM

[AAC+04] Yuri Akutin, Cristina Anderson, Marius Cornea, Alexey Ershov, Eugeny Gladkov, Evgeny Gvozdev, Bob Hanek, John Harrison, Alexander Isaev, Andrey Kolesov, Alexey Kovalev, Elena Luneva, Sergey Maidanov, Andrey Naraikin, Bob Norin, Pavel Shelepugin, Vladimir Sorokin, Shane Story, and Ping Tak Peter Tang. Highly optimized mathematical functions for the IA-64 architecture. Application note 245410-011, Intel Corporation, Santa Clara, CA, USA, December 16, 2004. 14 pp. URL `ftp://download.intel.com/software/opensource/numerics/libm.pdf`; `http://www.intel.com/cd/software/products/asmo-na/eng/219868.htm`; `http://www.intel.com/cd/software/products/asmo-na/eng/219871.htm?prn=y`.

August:1998:IPS

[ACM+98] David I. August, Daniel A. Connors, Scott A. Mahlke, John W. Sias, Kevin M. Crozier, Ben-Chung Cheng, Patrick R. Eaton, Qudus B. Olaniran, and Wen mei W. Hwu. Integrated predicated and speculative execution in the IMPACT EPIC architecture. In *Proceedings of the 25th annual international symposium on Computer architecture*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 1998. ISSN 0163-5964 (print), 1943-5851 (electronic). URL `http://delivery.acm.org/10.1145/280000/279391/p227-august.pdf`.

ACM:1999:PASa

[ACM99] ACM, editor. *Proceedings of the ACM SIGPLAN '99 Conference on Programming Language Design and Implementation (PLDI '99), Atlanta, Georgia, 2–4 May 1999*, volume 34(5) of *ACM SIGPLAN Notices*. ACM Press, New York, NY, USA, 1999. ISBN 1-58113-094-5. LCCN ????

ACM:2000:PIS

[ACM00] ACM, editor. *Proceedings of the International Symposium on*

Physical Design (ISPD-00), San Diego, CA, April 9–12, 2000. ACM Press, New York, NY, USA, 2000.

ACM:2001:SHP

[ACM01] ACM, editor. *SC2001: High Performance Networking and Computing. Denver, CO, November 10–16, 2001*. ACM Press and IEEE Computer Society Press, New York, NY, USA and 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2001. ISBN 1-58113-293-X. LCCN ????

ACM:2004:SHP

[ACM04a] ACM, editor. *SC 2004: High Performance Computing, Networking and Storage: Bridging communities: Proceedings of the IEEE/ACM Supercomputing 2004 Conference, Pittsburgh, PA, November 6–12, 2004*. ACM Press and IEEE Computer Society Press, New York, NY, USA and 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2004. ISBN 0-7695-2153-3. LCCN ????

August:2004:IPS

[ACM+04b] David I. August, Daniel A. Connors, Scott A. Mahlke, John W. Sias, Kevin M. Crozier, Ben-Chung Cheng, Patrick R. Eaton, Qudus B. Olaniran, and Wen mei W. Hwu. Integrated predicated and speculative execution in the IMPACT EPIC architecture. In DeGroot [DeG98], pages 227–237. ISBN 0-8186-8491-7. ISSN 0163-5964 (print), 1943-5851 (electronic). LCCN ???? URL `http://rogue.colorado.edu/draco/abstract.php?pub=impact.pub&paper_dir=papers; http://rogue.colorado.edu/draco/papers/isca-98-epic.pdf; http://rogue.colorado.edu/draco/papers/isca-98-epic.ps`.

ACM:2006:PCC

[ACM06] ACM, editor. *Proceedings of the 3rd conference on Computing Frontiers, May 3–5, 2006, Ischia, Italy*. ACM Press, New York, NY, USA, 2006. ISBN 1-59593-302-6. LCCN ???? ACM order number 104060.

Allan:2002:TRS

[AEJ+02] Alan Allan, Don Edenfeld, William H. Joyner, Jr., Andrew B. Kahng, Mike Rodgers, and Yervant Zorian. 2001 technology roadmap for semiconductors. *Computer*, 35(1):42–53, January 2002. CODEN CPTRB4. ISSN 0018-9162 (print), 1558-0814 (electronic). URL `http://dlib.computer.org/co/books/co2002/pdf/r1042.pdf; http://www.computer.org/computer/co2002/r1042abs.htm; http://www.intel.com/technology/silicon/alanallanieeecomputer0102.htm`.

Artigas:2000:ALT

[AGMM00] Pedro V. Artigas, Manish Gupta, Samuel P. Midkiff, and José E. Moreira. Automatic loop transformations and parallelization for Java. In ACM, editor,

Conference proceedings of the 2000 International Conference on Supercomputing: Santa Fe, New Mexico, May 8–11, 2000, pages 1–10. ACM Press, New York, NY, USA, 2000. ISBN 1-58113-270-0. LCCN ???? URL `http://delivery.acm.org/10.1145/340000/335232/p1-artigas.pdf`.

Aagaard:2000:TPH

[AH00] Mark Aagaard and John Harrison, editors. *Theorem Proving in Higher Order Logics, 13th International Conference, TPHOLs 2000, Portland, Oregon, USA, August 14–18, 2000, Proceedings*, volume 1869 of *Lecture Notes in Computer Science*. Springer-Verlag Inc., 2000. ISBN 3-540-67863-8. LCCN QA267.A1 L43 no.1869; QA76.9.A96 T655 200.

Aono:2000:AWI

[AK00] Fumio Aono and Masayuki Kimura. The AzusA 16-way Itanium server. *IEEE Micro*, 20(5):54–60, September/October 2000. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL `http://dlib.computer.org/mi/books/mi2000/pdf/m5054.pdf; http://www.computer.org/micro/mi2000/m5054abs.htm`.

Aamodt:2003:FMO

[AMC+03] Tor M. Aamodt, Pedro Marcuello, Paul Chow, Antonio González, Per Hammarlund, Hong Wang, and John P. Shen. A framework for modeling and optimization of prescient instruction prefetch. *ACM SIGMETRICS Performance Evaluation Review*, 31(1):13–24, June 2003. CODEN ???? ISSN 0163-5999 (print), 1557-9484 (electronic).

AMD:1999:ADN

[AMD99] AMD Corporation. AMD discloses new technologies at Microprocessor Forum — including x86 64-bit architecture and Lightning Data Transport^{TM}. Press release., October 5, 1999. URL `http://www.amd.com/news/prodpr/99105.html`.

AMD:2000:XTW

[AMD00] AMD Corporation. x86-64^{TM} technology white paper. Technical report, AMD Corporation, One AMD Place, Sunnyvale, CA 94088, USA, August 17, 2000. 12 pp. URL `http://www.amd.com/products/cpg/64bit/pdf/x86-64_wp.pdf; http://www1.amd.com/products/cpg/x8664bit/faq`.

AMD:2001:PIA

[AMD01] AMD Corporation, One AMD Place, Sunnyvale, CA 94088, USA. *Preliminary Information: AMD 64-Bit Technology: The AMD x86-64^{TM} Architecture Programmers Overview*, January 2001. 134 pp. URL `http://www.amd.com/products/cpg/64bit/pdf/x86-64_overview.pdf`.

Aditya:2000:CSM

[AMR00] Shail Aditya, Scott A. Mahlke, and B. Ramakrishna Rau. Code size minimization and retargetable assembly for custom EPIC and VLIW instruction formats. *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 5(4):752–773, January 2000. URL `http://www.acm.org/pubs/articles/journals/todaes/2000-5-4/p752-aditya/p752-aditya.pdf; http://www.acm.org/pubs/citations/journals/todaes/2000-5-4/p752-aditya/`.

Anonymous:1997:OI

[Ano97] Anonymous. Optimizing the IA-64. *IEEE Micro*, 17(5):6, September/October 1997. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

Anonymous:1998:HOM

[Ano98a] Anonymous. HP offers Merced deals. NetServer buyers to get discounts on IA-64 servers. *Information Week*, 682:34, May 18, 1998. CODEN INFWE4. ISSN 8750-6874.

Anonymous:1998:IPA

[Ano98b] Anonymous. IBM to port AIX to IA-64. vendor says Unix operating system will be ready when chip ships in 2000. *Information Week*, 697:24, August 24, 1998. CODEN INFWE4. ISSN 8750-6874.

Anonymous:1998:MNM

[Ano98c] Anonymous. Micro news: Merced update. *IEEE Micro*, 18(2):2, March/April 1998. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL `http://dlib.computer.org/dynaweb/mi/mi1998/@ebt-link; http://dlib.computer.org/mi/books/mi1998/pdf/m2002.pdf`.

Anonymous:1999:DNI

[Ano99a] Anonymous. Departments: News: Itanium, Athlon introduced; electronic paper. *IEEE Micro*, 19(6):2–??, November/December 1999. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

Anonymous:1999:HIC

[Ano99b] Anonymous. Hardware — IA-64-Cluster unter Linux — SGI demonstriert einen Server-Verbund auf Basis von Intels Itanium-Chips. *Computerwoche*, 26(48):39–40, 1999. ISSN 0170-5121.

Anonymous:1999:IAR

[Ano99c] Anonymous. IA-64 approaches reality. *Electronic Business*, 25 (12):10–12, ???? 1999. CODEN ELBUDL. ISSN 0163-6197.

Anonymous:1999:MNI

[Ano99d] Anonymous. Micro news: Intel unveils Itanium processor. *IEEE Micro*, 19(6):2, November/December 1999. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

URL `http://dlib.computer.org/mi/books/mi1999/pdf/m6002.pdf`.

Anonymous:1999:SII

[Ano99e] Anonymous. Special issue on Intel Architecture 64-bit (IA-64) technology. *Intel Technology Journal*, (Q4), November 22, 1999. URL `http://developer.intel.com/technology/itj/q41999.htm`.

Anonymous:19xx:TWI

[Anoxx] Anonymous. Top of the week — Intel's next step — the chipmaker's Itanium processor could fundamental alter the cost structure of business computing. *Information Week*, pages 22–25, 19xx. CODEN INFWE4. ISSN 8750-6874.

Anonymous:2000:CWS

[Ano00a] Anonymous. Compaq will skip Intel's Itanium chip for big servers, and move straight to its successors. *Computing (London 1980)*, page 6, March 9, 2000. CODEN CPTGB5. ISSN 0144-3097.

Anonymous:2000:FPF

[Ano00b] Anonymous. Forefront: Product features: Top UNIX server employs 64-way processor and prepares for the IA-64 Itanium CPU. *Electronic Design*, 48(22): 62–63, 2000. CODEN ELODAW. ISSN 0013-4872.

Anonymous:2000:HPS

[Ano00c] Anonymous. Hewlett–Packard setzt auf Linux — HP forciert die Portterung des Open-Source-Systems auf Intels Itanium und PA-Risc-CPUs. (German) [Hewlett–Packard sets up Linux — HP forces the porting of open-source systems to Intel's Itanium and PA-RISC CPUs]. *Computerwoche*, 27(2):26, ???? 2000. ISSN 0170-5121.

Anonymous:2000:IRK

[Ano00d] Anonymous. IA-64 — der RISC-Killer? — Intels Widersacher haben gute Chancen. (German) [IA-64 — the RISC killer? — Intel's opponent has good chances]. *Computerwoche*, 27(38):64–72, ???? 2000. ISSN 0170-5121.

Anonymous:2000:ICL

[Ano00e] Anonymous. IA-64-Cluster unter Linux — SGI demonstriert einen Server-Verbund auf Basis von Intels Itanium-Chips. (German) [IA-64 cluster under Linux — SGI demonstrates a server based on Intel' Itanium chips]. *Computerwoche*, 27(2): 26, ???? 2000. ISSN 0170-5121.

Anonymous:2000:IPG

[Ano00f] Anonymous. Intel processor gets Linux boost. TurboLinux demos software on Intel's forthcoming 64-bit Itanium chips. *Information Week*, 790:32, June 12, 2000. CODEN INFWE4. ISSN 8750-6874.

Anonymous:2000:IVS

[Ano00g] Anonymous. Itanium verspatet sich — Intels 64-Bit-Architektur kommt fruhestens im vierten

Quartal 2000, Rechner erst 2001. (German) [Itanium late — Intel's 64-bit architecture comes in the fourth quarter of 2000 at the earliest, the processor in 2001]. *Computerwoche*, 27(30): 4, ???? 2000. ISSN 0170-5121.

Anonymous:2000:LBW

[Ano00h] Anonymous. Linux beats Windows — open-source Trillian Linux will be ready for Intel's 64-bit Itanium processors. *Computer Shopper*, pages 254–255, June 2000. ISSN 0886-0556.

Anonymous:2000:LIS

[Ano00i] Anonymous. Linux: Mit IA-64 in den Server-Markt? — Erfolg hangt von Anwendungen ab. (German) [Linux: With IA-64 in the server market? — success hangs on its use]. *Computerwoche*, 27(38):75–78, ???? 2000. ISSN 0170-5121.

Anonymous:2000:NCF

[Ano00j] Anonymous. Neue Chancen für Intel-Server — Datenbanken profitieren von IA-64. (German) [new changes for Intel server — databases profit from IA-64]. *Computerwoche*, 27(38):62–63, ???? 2000. ISSN 0170-5121.

Anonymous:2000:NES

[Ano00k] Anonymous. New enterprise server choices. Intel's Itanium processor attracts interest as a platform for Unix apps. *Information Week*, 786:104, May 15, 2000. CODEN INFWE4. ISSN 8750-6874.

Anonymous:2000:NPAa

[Ano00l] Anonymous. New products: AVP for Linux/FreeBSD UNIX, Kaspersky Lab Ltd.; API PowerRAC Chassis 320, Alpha Processor Inc.; ODBC-ODBC Bridge, Easysoft Ltd.; LinkScan 6.1, Electronic Software Publishing Corporation; Metro-X Enhanced Server CD, Metro Link, Inc.; P-STAT Statistical Software, P-STAT, Inc.; System Manager in a Box v1.0, PegaSoft Canada; PGI Workstation 3.1, PGI; Quick Restore 2.6, Workstation Solutions, Inc.; Threads.h++ and Tools.h++ Professional, Rogue Wave Software; Scriptics Connect 1.0, 1.1, Scriptics Corporation; TapeWare 6.2 Backup Software, Yosemite Technologies, Inc.; DoubleVision for Linux Systems, Tridia Corporation. *Linux Journal*, 71:??, March 2000. CODEN LIJOFX. ISSN 1075-3583 (print), 1938-3827 (electronic).

Anonymous:2000:NPF

[Ano00m] Anonymous. New products: FileZerver, Microtest, Inc.; AT75C310, Aplio Inc.; Eyelet GUI, MoJo Designs Inc.; J2SE 1.2.2 for Linux, Sun Microsystems, Inc.; GNUPro Tools for IA-64, Red Hat Software; Linux edition of "A Mother's Shoah", IL NewMedia Publishing; +One Station, Maxspeed Corporation; Parallel Computing Toolkit, Wolfram Research; Rave Systems RackMount-

1UAXe, Rave Computer Association, Inc.; SafeWrite, TurnSafe Technologies, Inc.; Progress SonicMQ Adds Support for Linux, Progress Software Corporation; System Blocks, SM&A Corp.; T.Rex, Freemont Avenue Software, Inc.; Videomodem, COM One Services; SNA Gateway, Gcom, Inc.; Best Linux 2000, SOT Finnish Software Engineering Ltd. *Linux Journal*, 74:??, June 2000. CODEN LIJOFX. ISSN 1075-3583 (print), 1938-3827 (electronic).

Anonymous:2000:NNI

[Ano00n] Anonymous. News — NEC's 16 Itanium processor-based prototype IA-64 server running 64-bit SQL server on 64-bit Windows operating system. *Nippon Electric Company research and development*, 41(1):122, ???? 2000. CODEN NECRAU. ISSN 0048-0436; 0547-051X.

Anonymous:2000:SSC

[Ano00o] Anonymous. Server status: Compaq refuses Itanium. *Wall Street and Technology*, 18(5): 16–17, ???? 2000. CODEN WSTEE5. ISSN 1060-989X.

Anonymous:2000:TUS

[Ano00p] Anonymous. Top UNIX server employs 64-way processor and prepares for the IA-64 Itanium CPU. *Electronic Design*, 48(22): 62–63, ???? 2000. CODEN ELODAW. ISSN 0013-4872.

Anonymous:2001:BTL

[Ano01a] Anonymous. 64-bit technology: At long last Intel's Itanium processor has arrived to herald a mass-market future for 64-bit technology. *Personal computer world*, 24(2):144–148, ???? 2001. CODEN PCWODU. ISSN 0142-0232.

Anonymous:2001:TLL

[Ano01b] Anonymous. 64bit technology: At long last Intel's Itanium processor has arrived to herald a mass-market future for 64bit technology. *Personal computer world*, 16(9):144–148, 2001.

Anonymous:2001:BSI

[Ano01c] Anonymous. Bea setzt auf den Itanium — Die neue Intel-Plattform soll eine Alternative fur Weblogic auf Risc-Systemen bieten. *Computerwoche*, 28(32): 17, 2001. ISSN 0170-5121.

Anonymous:2001:DNI

[Ano01d] Anonymous. Departments: News: Intel introduces Itanium. tender offer extended again. show us your stuff. center spotlights STEP. use benchmark to compare hardware. image of the month. SIGGRAPH celebrates play. *Computer-aided engineering: CAE*, 20(7):10–??, 2001. CODEN CCAEDJ. ISSN 0733-3536.

Anonymous:2001:ESW

[Ano01e] Anonymous. Epic soll den Weg ebnen — Mit der Explicitly-Parallel-Instruction-Computing-

(Epic-) Architektur will Intel punkten. Eine breite Allianz von Hardware- und Softwareherstellern soll den Itanium ins Highend katapultieren. *Computerwoche*, 28(49):45, 2001. ISSN 0170-5121.

Anonymous:2001:ESL

[Ano01f] Anonymous. Express: Supercomputer auf Linux-Basis: 3300-Itanium-Prozessoren fur neuen Weltrekordrechner. *Elektronik*, 50(18):10–11, 2001. CODEN EKRKAR. ISSN 0013-5658.

Anonymous:2001:FLI

[Ano01g] Anonymous. First looks: The Itanium and 64-bit computing. *PC magazine: the independent guide to IBM-standard personal computing*, 20(16):28–33, 2001.

Anonymous:2001:FNI

[Ano01h] Anonymous. Forefront: News: Itanium processors will gang up to perform 13.6 teraflops. *Electronic Design*, 49(19):36–37, 2001. CODEN ELODAW. ISSN 0013-4872.

Anonymous:2001:HIB

[Ano01i] Anonymous. Herausforderer Itanium — Um in der 64-Bit-Welt erfolgreich zu sein, reicht der Chip allein nicht aus. Auch Compiler, Betriebssysteme und Applikationen mussen speziell angepasst werden. *Computerwoche*, 28(49):42–44, 2001. ISSN 0170-5121.

Anonymous:2001:IIW

[Ano01j] Anonymous. IBM Itanium workstation. *Personal computer world*, 16(9):62–63, 2001.

Anonymous:2001:ICS

[Ano01k] Anonymous. Intel call on the software industry to drum up interest in Itanium. *Computing*, 16(9):6–??, 2001.

Anonymous:2001:ILI

[Ano01l] Anonymous. Intel launches Itanium. *Library systems*, 21(7):3–??, 2001. ISSN 0277-0288.

Anonymous:2001:IEJ

[Ano01m] Anonymous. Itanium ab Ende Juni — Nach sieben Jahren Entwicklung und mit zwei Jahren Verspatung ist es nun soweit: Intel feiert leise das Prozessor-Debut seiner IA-64-Architektur. *Computerwoche*, 28(23):30, 2001. ISSN 0170-5121.

Anonymous:2001:IAP

[Ano01n] Anonymous. Itanium ante portas — Am 29. Mai kommen die 64-Bit-CPUs in Stuckzahlen auf den Markt. *Computerwoche*, 28 (20):6, 2001. ISSN 0170-5121.

Anonymous:2001:IES

[Ano01o] Anonymous. Itanium-Entwicklung stockt. *Computerwoche*, 28(11): 48–51, 2001. ISSN 0170-5121.

Anonymous:2001:LMI

[Ano01p] Anonymous. Linux not mentioned in Itanium article. *Li-*

brary systems, 21(9):6–??, 2001. ISSN 0277-0288.

Anonymous:2001:IWI

[Ano01q] Anonymous. Mit dem Itanium will Intel in der High-end-Server-Arena Fuss fassen. Nach dem Ruckzug von Compaq und HP bleiben Sun und IBM als Konkurrenten. *Computerwoche*, 28(30):16–17, 2001. ISSN 0170-5121.

Anonymous:2001:NES

[Ano01r] Anonymous. New enterprise server choices: Intel's Itanium processor attracts interest as a platform for Unix apps. *Information Week*, 21(1):104–110, 2001. CODEN INFWE4. ISSN 8750-6874.

Anonymous:2001:NPP

[Ano01s] Anonymous. New products: PowerEdge adopts Intel Itanium processors. cA blocks malicious code. *Network magazine: the competitive edge in business technology*, 16(9):80–81, 2001.

Anonymous:2001:NNP

[Ano01t] Anonymous. News: NEC provided 16-way Itanium server "AzusA" for Hewlett–Packard as an OEM products. *Nippon Electric Company research and development*, 42(1):91, 2001. CODEN NECRAU. ISSN 0048-0436; 0547-051X.

Anonymous:2001:NEI

[Ano01u] Anonymous. Notizen — Einblick: Itanium — ein "heisser" Tip fur Server? *Elektronik*, 50(19):28–29, 2001. CODEN EKRKAR. ISSN 0013-5658.

Anonymous:2001:PIM

[Ano01v] Anonymous. Pipeline: Intel's McKinley chip shows its face. A sea creature boosts optical networking. CEO pay and worker pay are diverging. AOL, EarthLink helped FBI find terrorists. *PC Magazine*, 20(18):29, ???? 2001.

Anonymous:2001:SSC

[Ano01w] Anonymous. Server status: Compaq refuses Itanium. *Wall Street and Technology*, 16(9):16–17, 2001. CODEN WSTEE5. ISSN 1060-989X.

Anonymous:2001:SRS

[Ano01x] Anonymous. Steckt Risc in der Sackgasse? — Der Wettbewerb wird harter. Leistungssteigerungen mussen die Risc-Anbieter teuer erkaufen. Deshalb hat sich Compaq zur Aufgabe der Alpha-Architektur und zum Umstieg auf Itanium entschieden. *Computerwoche*, 28(49):8–13, 2001. ISSN 0170-5121.

Anonymous:2001:TAA

[Ano01y] Anonymous. Tech analyzer: AMD wields 64-bit hammer: Chipmaker's new Hammer CPU is likely to cost less and offer better backward compatibility than Intel's Itanium processor. *Information Week*, 28(23):64–68, 2001. CODEN INFWE4. ISSN 8750-6874.

Anonymous:2001:WSM

[Ano01z] Anonymous. A Windows for supercomputing: Microsoft is quietly launching an OS to handle Intel's new, 64-bit Itanium CPU. *PC world*, 19(8):58–65, 2001.

Anonymous:2002:ASI

[Ano02a] Anonymous. From AlphaServer systems to the Intel Itanium architecture a bright future for OpenVMS system management. White paper, Hewlett–Packard Corporation, Palo Alto, CA, USA, 2002. URL `http://sysdoc.doors.ch/HP/OpenVMS_Itanium_system_management.pdf`.

Anonymous:2002:III

[Ano02b] Anonymous. Inside the Intel Itanium 2 processor. White paper, Hewlett–Packard Corporation, Palo Alto, CA, USA, July 2002. URL `http://www.dig64.org/about/Itanium2_white_paper_public.pdf`.

Anonymous:2002:OFP

[Ano02c] Anonymous. OpenVMS floating-point arithmetic on the Itanium architecture. Technical report, Hewlett–Packard Corporation, Palo Alto, CA, USA, September 2002. URL `http://sysdoc.doors.ch/HP/openvms_ipf_floating_point_wp.pdf`.

Anonymous:2002:OAI

[Ano02d] Anonymous. Optimizing applications with the Intel C++ and Fortran compilers for Windows and Linux. Technical report, Hewlett–Packard Corporation, Palo Alto, CA, USA, 2002. URL `http://www.intel.com/software/products/compilers/c60/techtopics/Compiler_Optimization_6.pdf`.

Anonymous:2003:CRN

[Ano03] Anonymous, editor. *5th Conference on Real Numbers and Computers 2003 — RNC5, Lyon, France, September 2003*. ????, ????, 2003. ISBN ???? LCCN ????

Anonymous:2004:IIP

[Ano04] Anonymous. Intel Itanium processor family reference guide: IA-32 execution layer. Web document., 2004. URL `http://download.intel.com/design/Itanium/Downloads/25431803.pdf`.

Anonymous:2006:PGI

[Ano06] Anonymous, editor. *Proceedings of Gelato ICE: Itanium Conference and Expo: Spotlighting Linux on Itanium-based Platforms, October 1–4, 2006, Biopolis, Singapore*, 2006. ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/; http://www.ice.gelato.org/about/oct06_presentations.php`.

Anwar:2006:SNG

[Anw06] Arif Anwar. SynaBASE: Next-generation bioinformatics database platform. In Anonymous [Ano06], page ?? ISBN

???? LCCN ???? URL http://www.ice.gelato.org/ ; http://www.ice.gelato.org/about/oct06_presentations.php.

Avetisyan:2006:IRA

[Ave06] Arutyun I. Avetisyan. The ISP RAS activities for improving GCC for Itanium. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_gccimprov_avetisyan_ispras.pdf.

Anderson:2002:CCS

[AWB02] Ferd E. Anderson, J. Steve Wells, and Eugene Z. Berta. The core clock system on the next generation Itanium^{TM} microprocessor. In IEEE [IEE02], page ?? ISBN ???? ISSN 0743-1686. LCCN ???? URL http://cpus.hp.com/technical_references/isscc_2002/isscc_2002_6.shtml.

Beck:2002:POA

[BBC+02] Will Beck, Glenn Bowles, Drew Comstock, Gaitan D'Antoni, and Jim Parker. Porting OpenVMS applications to Intel Itanium architecture. White paper, Hewlett–Packard Corporation, Palo Alto, CA, USA, April 2002. URL http://sysdoc.doors.ch/HP/OpenVMS_IPF_PORTING_WP.pdf.

Blau:2001:NAE

[BBS+01] J. Blau, S. Barlas, V. Singh, L. Geppert, H. Goldstein, S. K. Moore, M. J. Riezenman, and S. Miller. News analysis: (1) Europe's cellulars to share infrastructure? (2) Why the fuss about 3G? (3) Senate changes will shake telecom, defense R&D, Energy. (4) In Energy, will Bingaman out-Cheney Cheney? (5) India's power grid finds helping hand. (6) The Itanium platform lands its first computing systems. (7) Ion beam keeps liquid crystals in line. (8) How to raise UV nanolasers. (9) Swedish start-up puts new spin on pen and paper. (10) Big welcome for MIT's Web-based courseware. *IEEE Spectrum*, 38(7):20–37, July 2001. CODEN IEESAM. ISSN 0018-9235 (print), 1939-9340 (electronic).

Brifault:2004:DCM

[BC04] K. Brifault and H. P. Charles. Data cache management on EPIC architecture: optimizing memory access for image processing. *ACM SIGARCH Computer Architecture News*, 32(3): 35–42, June 2004. CODEN CANED2. ISSN 0163-5964 (print), 1943-5851 (electronic).

Bharadwaj:2000:IIC

[BCC+00] Jay Bharadwaj, William Y. Chen, Weihaw Chuang, Gerolf Hoflehner, Kishore Menezes, Kalyan Muthukumar, and Jim

Pierce. The Intel IA-64 compiler code generator. *IEEE Micro*, 20(5):44–53, September/October 2000. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL `http://dlib.computer.org/mi/books/mi2000/pdf/m5044.pdf`; `http://www.computer.org/micro/mi2000/m5044abs.htm`.

Blickstein:1992:GOC

[BCD+92] David S. Blickstein, Peter W. Craig, Caroline S. Davidson, R. Neil Faiman, Jr., Kent D. Glossop, Richard B. Grove, Steven O. Hobbs, and William B. Noyce. The GEM optimizing compiler system. *Digital Technical Journal of Digital Equipment Corporation*, 4(4):121–136, Fall 1992. CODEN DTJOEL. ISSN 0898-901X. URL `ftp://ftp.digital.com/pub/Digital/info/DTJ/v4n4/The_GEM_Optimizing_Compiler_Sy_01apr1993DTJ808PS.ps`; `http://www.digital.com:80/info/DTJ808/DTJ808SC.TXT`.

Baraz:2004:IEL

[BDE+04] Leonid Baraz, Tevi Devor, Orna Etzion, Shalom Goldenberg, Alex Skaletsky, Yun Wang, and Yigal Zemach. IA-32 execution layer: a two-phase dynamic translator designed to support IA-32 applications on Itanium-based systems. Technical report, Hewlett–Packard Corporation, Palo Alto, CA, USA, 2004. URL `http://www.intel.com/cd/ids/developer/asmo-na/eng/93086.htm`.

Barroso:2000:PSA

[BGM+00] Luiz André Barroso, Kourosh Gharachorloo, Robert McNamara, Andreas Nowatzyk, Shaz Qadeer, Barton Sano, Scott Smith, Robert Stets, and Ben Verghese. Piranha: a scalable architecture based on single-chip multiprocessing. In *Proceedings of the 27th Annual International Symposium on Computer Architecture: June 12–14, 2000, Vancouver, British Columbia*. ACM Press, New York, NY, USA, 2000. ISBN 1-58113-232-8. ISSN 0163-5964 (print), 1943-5851 (electronic). LCCN QA76.9.A73 S97 2000. URL `http://delivery.acm.org/10.1145/340000/339696/p282-barroso.pdf`.

Buck:2004:DCC

[BH04] Bryan R. Buck and Jeffrey K. Hollingsworth. Data centric cache measurement on the Intel Itanium 2 processor. In ACM [ACM04a], page 58. ISBN 0-7695-2153-3. LCCN ????

Brooks:2000:VBC

[BM00] David Brooks and Margaret Martonosi. Value-based clock gating and operation packing: dynamic strategies for improving processor power and performance. *ACM Transactions on Computer Systems*, 18(2): 89–126, May 2000. CODEN ACSYEC. ISSN 0734-2071

(print), 1557-7333 (electronic). URL http://www.acm.org/pubs/citations/journals/tocs/2000-18-2/p89-brooks/.

Boldo:2005:SFC

[BM05] Sylvie Boldo and Jean-Michel Muller. Some functions computable with a fused-mac. In IEEE [IEE05], page ?? ISBN ???? LCCN ???? URL http://arith17.polito.it/final/paper-106.pdf.

Bharadwaj:1999:WSP

[BMM99] J. Bharadwaj, K. Menezes, and C. McKinsey. Wavefront scheduling: path based data representation and scheduling of subgraphs. In IEEE, editor, *Proceedings: 32nd Annual International Symposium on Microarchitecture: Haifa, Israel, November 16–18, 1999*, pages 262–271. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 1999. ISBN 0-7695-0437-X. LCCN QA76.6.I5736 1999. URL http://ieeexplore.ieee.org/iel5/6577/17552/00809464.pdf. IEEE Computer Society order number PR0043.

Bradley:2002:SCR

[BMS02] David Bradley, Patrick Mahoney, and Blaine Stackhouse. The 16kB single-cycle read access cache on a next generation 64b Itanium microprocessor. In IEEE [IEE02], page ?? ISBN ???? ISSN 0743-1686. LCCN ???? URL http://cpus.hp.com/technical_references/isscc_2002/isscc_2002_3.shtml.

Bohr:1998:STL

[Boh98] Mark Bohr. Silicon trends and limits for advanced microprocessors. *Communications of the ACM*, 41(3):80–87, March 1998. CODEN CACMA2. ISSN 0001-0782 (print), 1557-7317 (electronic). URL http://delivery.acm.org/10.1145/280000/272327/p80-bohr.pdf; http://www.acm.org:80/pubs/citations/journals/cacm/1998-41-3/p80-bohr/.

Bohr:2002:INT

[Boh02] Mark Bohr. Intel's 90 nm technology: Moore's Law and more. Technical report, Hewlett–Packard Corporation, Palo Alto, CA, USA, 2002. URL http://www.intel.com/research/silicon/micron.htm.

Brender:2002:BPL

[Bre02] Ronald F. Brender. The BLISS programming language: a history. *Software—Practice and Experience*, 32(10):955–981, August 2002. CODEN SPEXBL. ISSN 0038-0644 (print), 1097-024X (electronic). URL http://www3.interscience.wiley.com/cgi-bin/abstract/96516179/START; http://www3.interscience.wiley.com/cgi-bin/fulltext?ID=96516179&PLACEBO=IE.pdf.

CC:2003:UPI

[Cam03] Cambridge Consulting. UltraSPARC's prospects in an Itanium world: a comparative analysis of ultraSPARC and Itanium architectures, performance attributes, and roadmaps for the future. World-Wide Web document., May 30, 2003. URL `http://h71028.www7.hp.com/ERC/downloads/CambridgeUltraSPARC_v6.pdf`.

Chandrakasan:2001:DHP

[CBF01] Anantha Chandrakasan, William J. Bowhill, and Frank Fox. *Design of high-performance microprocessor circuits*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2001. ISBN 0-7803-6001-X. xx + 557 pp. LCCN TK7895.M5 D47 2001. US$125.00. URL `http://shop.ieee.org/store/product.asp?prodno=PC5836`. IEEE order no. PC5836.

Catthoor:2000:HSC

[CDK00] Francky Catthoor, Nikil D. Dutt, and Christoforos E. Kozyrakis. How to solve the current memory access and data transfer bottlenecks at the processor architecture or at the compiler level. In *Design, Automation, and Test in Europe Conference and Exhibition 2000: proceedings, Paris, France, March 27–30, 2000*, pages 426–435. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2000. ISBN 1-58113-244-1; 0-7695-0537-6, 0-7695-0538-4 (casebound), 0-7695-0539-2 (microfiche). LCCN ???? URL `http://delivery.acm.org/10.1145/350000/343813/p426-catthoor.pdf`.

Carter:2000:LCP

[CF00] Larry Carter and Jeanne Ferrante, editors. *Languages and compilers for parallel computing: 12th International Workshop, LCPC'99, La Jolla, CA, USA, August 4–6, 1999; proceedings*, volume 1863 of *Lecture Notes in Computer Science*. Springer-Verlag Inc., New York, NY, USA, 2000. ISBN 3-540-67858-1. ISSN 0302-9743 (print), 1611-3349 (electronic). LCCN QA76.58 .L36 2000.

Carver:1999:POS

[CFLZ99] Kathy Carver, Chuck Fleckenstein, Joshua LeVasseur, and Stephan Zeisset. Porting operating system kernels to the IA-64 architecture for presilicon validation purposes. *Intel Technology Journal*, (Q4): 7, November 22, 1999. ISSN 1535-766X. URL `http://developer.intel.com/technology/itj/q41999/articles/art_4.htm`; `http://developer.intel.com/technology/itj/q41999/pdf/porting.pdf`.

Carlson:2003:IRB

[CH03] Jim Carlson and Jerry Huck. *Itanium rising: breaking through Moore's second law of comput-*

ing power. Prentice-Hall PTR, Upper Saddle River, NJ 07458, USA, 2003. ISBN 0-13-046415-5. xx + 198 pp. LCCN QA76.9.A73 C365 2003.

Chatterjee:2006:BML

[Cha06] Soumitra Chatterjee. 64-bit migration to Linux on Itanium: Challenges, advantages, and tools. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/; http://www.ice.gelato.org/about/oct06_presentations.php`.

Cornea:2003:DSR

[CHI+03] M. Cornea, J. Harrison, C. Iordache, B. Norin, and S. Story. Division, square root and remainder algorithms for the Intel Itanium architecture. Report, Intel Corporation, Santa Clara, CA, USA, November 2003.

Cornea-Hasegan:1999:IFP

[CHN99] Marius Cornea-Hasegan and Bob Norin. IA-64 floating-point operations and the IEEE standard for binary floating-point arithmetic. *Intel Technology Journal*, (Q4):16, November 22, 1999. URL `http://developer.intel.com/technology/itj/q41999/articles/art_6.htm; http://developer.intel.com/technology/itj/q41999/pdf/ia64fpbf.pdf`.

Christy:1996:IMW

[Chr96] Peter Christy. IA-64 and Merced — what and why. *Microprocessor Report*, 10(17):17–19, December 30, 1996. ISSN 0899-9341. URL `http://www.cs.cmu.edu/afs/cs.cmu.edu/academic/class/15740-f00/public/doc/discussions/uniprocessors/ia64/mpr_merced_whats_new_dec96.ps.gz`.

Cornea:2002:SCI

[CHT02] Marius Cornea, John Harrison, and Ping Tak Peter Tang. *Scientific computing on Itanium-based systems*. Intel Corporation, Santa Clara, CA, USA, 2002. ISBN 0-9712887-7-1. xvii + 406 pp. LCCN ???? US$69.95. URL `http://www.intel.com/intelpress/sum_scientific.htm`.

Chubb:2006:GS

[Chu06a] Peter Chubb. The GPT and superpages. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_superpages_chubb_unsw.pdf`.

Chubb:2006:VUL

[Chu06b] Peter Chubb. Virtualization and user-level drivers. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_vm_chubb_unsw.pdf`.

Chung:2006:COA

[Chu06c] Shin Yee Chung. ClustalW optimization: Adaptive scheduling. In Anonymous [Ano06],

page ?? ISBN ???? LCCN ???? URL http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_clustalwaddon_chung_ihpc.pdf; http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_clustalwperf_chung_ihpc.pdf.

Collard:2003:OPC

[CL03] Jean-François Collard and Daniel Lavery. Optimizations to prevent cache penalties for the Intel Itanium 2 processor. In IEEE [IEE03], pages 105–114. ISBN 0-7695-1913-X. LCCN ???? ACM Order No. 530033.

Clabby:2006:HIA

[Cla06] Joe Clabby. The HP Itanium architecture decision. Internet video program., October 24, 2006. URL http://itw.itworld.com/GoNow/a30051a154506a382798246a0.

Cierniak:2000:PJJ

[CLS00] Michał Cierniak, Guei-Yuan Lueh, and James M. Stichnoth. Practicing JUDO: Java under dynamic optimizations. *ACM SIGPLAN Notices*, 35(5):13–26, May 2000. CODEN SINODQ. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic). URL http://www.acm.org/pubs/articles/proceedings/pldi/349299/p13-cierniak/p13-cierniak.pdf; http://www.acm.org/pubs/citations/proceedings/pldi/349299/p13-cierniak/.

Charney:2001:UJO

[CMM01] Reginald Charney, Don Marti, and Gary A. Messenbrink. upFRONT: Job opening trends; the kernel speaks; win on lin on thin; LJ index — March 2001; Linux bytes other markets: Bay Area Rapid Transit (BART): Under control with Linux; stop the presses: Kylix clix with CLX. *Linux Journal*, 84:8, 10, 12, 14, April 2001. CODEN LIJOFX. ISSN 1075-3583 (print), 1938-3827 (electronic).

Colwell:2005:PCP

[Col05] Robert P. Colwell. *The Pentium Chronicles: The People, Passion, and Politics Behind Intel's Landmark Chips*. Wiley, New York, NY, USA, 2005. ISBN 0-471-73617-1. xix + 187 pp. LCCN ???? US$24.95.

Crawford:2000:GEI

[Cra00] John H. Crawford. Guest Editor's introduction: Introducing the Itanium processors. *IEEE Micro*, 20(5):9–11, September/October 2000. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL http://dlib.computer.org/mi/books/mi2000/pdf/m5009.pdf; http://www.computer.org/micro/mi2000/m5009abs.htm.

Chou:2000:IPC

[CS00] Yuan Chou and John Paul Shen. Instruction path coprocessors. In *The 27th Annual International Symposium on Com-*

puter architecture, pages 270–281. ACM Press, New York, NY, USA, 2000. ISSN 0163-5964 (print), 1943-5851 (electronic). URL `http://delivery.acm.org/10.1145/340000/339694/p270-chou.pdf`.

Chen:2008:SSP

[CWY+08] Haibo Chen, Xi Wu, Liwei Yuan, Binyu Zang, Pen chung Yew, and Frederic T. Chong. From speculation to security: Practical and efficient information flow tracking using speculative hardware. *ACM SIGARCH Computer Architecture News*, 36 (3):401–412, June 2008. CODEN CANED2. ISSN 0163-5964 (print), 1943-5851 (electronic).

Djoudi:2005:MMA

[DBC+05] Lamia Djoudi, Denis Barthou, Patrick Carribault, Christophe Lemuet, Jean-Thomas Acquaviva, and William Jalby. MAQAO: Modular assembler quality analyzer and optimizer for Itanium 2. In ????, editor, *The 4th Workshop on EPIC architectures and compiler technology, San Jose, CA, USA*, volume 200, page 20. ????, ????, 2005. URL `https://hal.archives-ouvertes.fr/hal-00141075/en/; https://www.labri.fr/perso/barthou/ps/maqao.pdf`.

Demshki:2000:DII

[DBWA00] Michael Demshki, Melvin Benedict, Dong Wei, and Tomm Aldridge. Designing interoperability into IA-64 systems: DIG64 guidelines. Technical report, Intel Corporation, Santa Clara, CA, USA, 2000. 56 pp. URL `http://developer.intel.com/design/ia-64/idfdIG2/`.

deDinechin:2000:CEHb

[dD00a] Christophe de Dinechin. C++ exception handling. *IEEE Concurrency*, 8(4):72–79, October/December 2000. CODEN IECMFX. ISSN 1092-3063 (print), 1558-0849 (electronic). URL `http://dlib.computer.org/pd/books/pd2000/pdf/p4072.pdf; http://www.computer.org/concurrency/pd2000/p4072abs.htm`.

deDinechin:2000:CEHa

[dD00b] Christophe de Dinechin. C++ exception handling for IA64. In USENIX [USE00], page ?? ISBN 1-880446-15-4. LCCN QA76.76.S95 W67 2000. URL `http://www.usenix.org/publications/library/proceedings/osdi2000/wiess2000/dinechin.html`.

deDinechin:2004:FCR

[dDDL04] Florent de Dinechin, David Defour, and Christoph Lauter. Fast correct rounding of elementary functions in double precision using double-extended arithmetic. Research Report RR2004-10, École Normale Supérieure de Lyon, 69364 Lyon Cedex 07, France, March 2004. 2 + 12 pp. URL `http://www.ens-`

lyon.fr/LIP/Pub/Rapports/RR/RR2004/RR2004-10.pdf.

DeRose:2006:EXI

[De 06] César De Rose. Evaluating Xen IA-64 security and performance. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_xeneval_derose_pucrs.pdf.

DeGroot:1998:PIS

[DeG98] Doug DeGroot, editor. *Proceedings of the 25th International Symposium on Computer Architecture, Barcelona, Spain, June 27–July 02, 1998*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 1998. ISBN 0-8186-8491-7. ISSN 0163-5964 (print), 1943-5851 (electronic). LCCN ????

Dahlen:2000:SWC

[DGMM00] Eric Dahlen, Jennifer Gustin, Susan Meredith, and Doug Moran. The 82460GX server/workstation chip set. *IEEE Micro*, 20(6):69–75, November/December 2000. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL http://dlib.computer.org/mi/books/mi2000/pdf/m6069.pdf; http://www.computer.org/micro/mi2000/m6069abs.htm.

Driesen:1998:AIB

[DH98] Karel Driesen and Urs Hölzle. Accurate indirect branch prediction. In *Proceedings of the 25th annual international symposium on Computer architecture*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 1998. ISSN 0163-5964 (print), 1943-5851 (electronic). URL http://delivery.acm.org/10.1145/280000/279380/p167-driesen.pdf.

Diefendorff:1999:PFM

[Die99] Keith Diefendorff. Power4 focuses on memory bandwidth: IBM confronts IA-64, says ISA not important. *Microprocessor Report*, 13(13):??, October 6, 1999. ISSN 0899-9341.

Dulong:1999:OII

[DKK+99] Carole Dulong, Rakesh Krishnaiyer, Dattatraya Kulkarni, Daniel Lavery, Wei Li, John Ng, and David Sehr. An overview of the Intel IA-64 compiler. *Intel Technology Journal*, (Q4):15, November 22, 1999. URL http://developer.intel.com/technology/itj/q41999/articles/art_1.htm; http://developer.intel.com/technology/itj/q41999/pdf/compiler.pdf.

Doshi:2001:OSD

[DKM01] G. Doshi, R. Krishnaiyer, and K. Muthukumar. Optimizing software data prefetches with rotating registers. In IEEE, editor, *2001 International Conference on Parallel Architectures and Compilation Techniques:*

proceedings: 8–12 September, 2001, Barcelona, Catalunya, Spain, pages x + 305. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2001. ISBN 0-7695-1363-8. LCCN QA76.58.I553 2001. URL `http://ieeexplore.ieee.org/lpdocs/epic03/`.

Dong:2006:XIV

[Don06] Yaozu Dong. Xen and Intel virtualization technology for IA-64. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_xenvt_dong_intel.pdf`.

Doran:1999:EFI

[Dor99] Mark Doran. Extensible Firmware Interface: booting the new generation of Intel Architecture platforms. Technical report, Intel Corporation, Santa Clara, CA, USA, September 1, 1999. 45 pp. URL `http://developer.intel.com/design/ia-64/downloads/IDFEFI.htm`.

Doshi:1999:UIA

[Dos99] Gautam Doshi. Understanding the IA-64 architecture. Technical report, Intel Corporation, Santa Clara, CA, USA, August 31, 1999. 65 pp. URL `http://developer.intel.com/design/ia-64/idfisa/index.htm`.

Dove:1999:PAI

[Dov99] Ken Dove. Programmatic advantages of IA-64 for large systems. *UNIX Review*, 17(10): 34–36, ???? 1999. CODEN UNRED5. ISSN 0742-3136.

Dulong:2001:MCI

[DSR01] Carole Dulong, Priti Shrivastav, and Azita Refah. The making of a compiler for the Intel(R) Itanium processor. *Intel Technology Journal*, (Q3): 7, August 1, 2001. ISSN 1535-766X. URL `http://developer.intel.com/technology/itj/q32001/articles/art_4.htm`; `http://developer.intel.com/technology/itj/q32001/pdf/art_4.pdf`.

Desai:2000:IPC

[DTZR00] U. Desai, S. Tam, R. Kim. J. Zhang, and S. Rusu. Itanium processor clock design. In ACM [ACM00], pages 94–98.

Dulong:1998:IAW

[Dul98] Carole Dulong. The IA-64 architecture at work. *Computer*, 31(7):24–32, July 1998. CODEN CPTRB4. ISSN 0018-9162 (print), 1558-0814 (electronic). URL `http://dlib.computer.org/co/books/co1998/pdf/r7024.pdf`; `http://www.computer.org/computer/co1998/r7024abs.htm`.

Engels:2001:PPS

[EFKR01] Daniel W. Engels, Jon Feldman, David R. Karger, and

Matthias Ruhl. Parallel processor scheduling with delay constraints. In *Twelfth Annual Symposium on Discrete algorithms*, pages 577–585. ACM Press, New York, NY, USA, 2001. ISBN 0-89871-490-7. LCCN ???? URL `http://delivery.acm.org/10.1145/370000/365538/p577-engels.pdf`.

Eranian:2000:LIP

[EM00] Stéphane Eranian and David Mosberger. The Linux/ia64 project: Kernel design and status report. Technical Report HPL-2000-85, Hewlett–Packard Corporation, Palo Alto, CA, USA, 2000. URL `http://www.hpl.hp.com/techreports/`.

Eichenberger:2000:IAA

[EMM00] Alexandre Eichenberger, Waleed Meleis, and Suman Maradani. An integrated approach to accelerate data and predicate computations in hyperblocks. In *Proceedings of the 33rd annual IEEE/ACM international symposium on Microarchitecture*. ACM Press, New York, NY, USA, 2000. ISBN 1-58113-196-8. LCCN ???? URL `http://delivery.acm.org/10.1145/370000/360140/p101-eichenberger.pdf`.

English:2000:MNIb

[Eng00] Marie English. Micro news: Intel releases Itanium guide. *IEEE Micro*, 20(3):3, May/June 2000. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL `http://dlib.computer.org/mi/books/mi2000/pdf/m3003.pdf`.

Eranian:2006:UPI

[Era06] Stéphane Eranian. Update on the Perfmon2 interface. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_perfmon2_eranian_hp.pdf`.

Evans:2003:IAP

[ET03] James S. Evans and Gregory L. Trimper. *Itanium architecture for programmers: understanding 64-bit processors and EPIC principles*. Prentice-Hall, Upper Saddle River, NJ 07458, USA, 2003. ISBN 0-13-101372-6. xxxiv + 529 pp. LCCN QA76.8.I83 E83 2003.

Fang:1999:CTI

[Fan99] Jesse Fang. Compiler technology on IA-64. In IEEE [IEE99], page ?? ISBN ???? LCCN ???? URL `http://www.hotchips.org/hotc11_index.html`.

Faraboschi:2000:LTP

[FBF+00] Paolo Faraboschi, Geoffrey Brown, Joseph A. Fisher, Giuseppe Desoli, and Fred Homewood. Lx: a technology platform for customizable VLIW embedded processing. In *The 27th Annual International Symposium on Computer architecture 2000*, ACM

SIGARCH Computer Architecture News, pages 203–213. ACM Press, New York, NY, USA, 2000. ISSN 0163-5964 (print), 1943-5851 (electronic). URL `http://delivery.acm.org/10.1145/340000/339682/p203-faraboschi.pdf`.

Fleckenstein:1999:POS

[FCLZ99] Chuck Fleckenstein, Kathy Carver, Joshua LeVasseur, and Stephan Zeisset. Porting operating system kernels to the IA-64 architecture for pre-silicon validation purposes. *Intel Technology Journal*, (Q4):7, November 22, 1999. URL `http://developer.intel.com/technology/itj/q41999/articles/art_4.htm`; `http://developer.intel.com/technology/itj/q41999/pdf/porting.pdf`.

Fisher:2005:ECV

[FFY05] Joseph A. Fisher, Paolo Faraboschi, and Clifford Young. *Embedded computing: a VLIW approach to architecture, compilers and tools*. Morgan Kaufmann Publishers, San Francisco, CA, USA, 2005. ISBN 1-55860-766-8 (hardcover). xxxiii + 671 pp. LCCN TK7895.E42 F57 2005; TK7895.E42 F57 2005.

Fisher:1979:OHM

[Fis79] Joseph Allen Fisher. *The Optimization of Horizontal Microcode With and Beyond Basic Blocks: An Application of Processor Scheduling with Resources*. Ph.D. dissertation, Courant Institute, New York University, New York, NY, USA, October 1979. v + 174 pp. URL `http://wwwlib.umi.com/dissertations/dlnow/8010348`.

Fisher:1983:VLI

[Fis83] Joseph A. Fisher. Very long instruction word architectures and the ELI-512. In *Proceedings of the 10th Annual International Symposium on Computer Architectures, Stockholm, Sweden*, volume 11(3) of *SIGARCH Newsletter: Computer Architecture*, pages 140–150. ACM Press, New York, NY, USA, 1983. ISBN 0-89791-101-6. ISSN 0884-7495. LCCN QA76.9.A73S9a. Reprinted in [Fis98].

Fisher:1998:VLI

[Fis98] Joseph A. Fisher. Very long instruction word architectures and the ELI-512. In Gurindar Sohi, editor, *25 years of the International Symposia on Computer Architecture (selected papers), Barcelona, Spain*, pages 263–273. ACM Press, New York, NY, USA, 1998. ISBN 1-58113-058-9. LCCN QA76.9.A73. Reprint of [Fis83].

Fetzer:2002:FBI

[FO02] Eric S. Fetzer and John T. Orton. A fully-bypassed 6-issue integer datapath and register file on an Itanium microprocessor. In IEEE [IEE02], page ?? ISBN ???? ISSN 0743-1686. LCCN ???? URL `http://cpus.hp.`

com/technical_references/isscc_2002/isscc_2002_2.shtml.

Fowler:1999:N

[Fow99] Dennis Fowler. Netnews. *net-Worker*, 3(2):7–11, June 1999. ISSN 1091-3556. URL http://delivery.acm.org/10.1145/310000/302501/p7-fowler.pdf.

Flautner:2000:TLP

[FURM00a] Krisztián Flautner, Rich Uhlig, Steve Reinhardt, and Trevor Mudge. Thread level parallelism and interactive performance of desktop applications. *ACM SIGPLAN Notices*, 35(11):129–138, November 2000. CODEN SINODQ. ISBN 1-58113-317-0. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic). URL http://delivery.acm.org/10.1145/360000/357001/p129-flautner.pdf.

Flautner:2000:TLPb

[FURM00b] Krisztián Flautner, Rich Uhlig, Steve Reinhardt, and Trevor Mudge. Thread level parallelism and interactive performance of desktop applications. *ACM SIGPLAN Notices*, 35(11):129–138, November 2000. CODEN SINODQ. ISBN 1-58113-317-0. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic). URL http://delivery.acm.org/10.1145/360000/357001/p129-flautner.pdf.

Garber:1997:NBJ

[GC97] Lee Garber and David Clark. News briefs: Judge rejects US restrictions on export of encryption; Intel, HP unveil Merced chip; Java wars heat up; AOL acquires CompuServe subscribers; confusion in the DVD marketplace; 'amazing grace' heads to sea; PC firms back down on convergence; business use will drive Internet growth; company offers $1-million prize for hackers. *Computer*, 30(11):22–25, November 1997. CODEN CPTRB4. ISSN 0018-9162 (print), 1558-0814 (electronic). URL http://pdf.computer.org/co/books/co1997/pdf/ry022.pdf.

Grun:2000:MAC

[GDN00] Peter Grun, Nikil Dutt, and Alex Nicolau. Memory aware compilation through accurate timing extraction. In ACM, editor, *Proceedings 2000: Design Automation Conference, 37th, Los Angeles Convention Center, Los Angeles, CA, June 5–9, 2000*, pages 316–321. ACM Press, New York, NY, USA, 2000. ISBN 1-58113-187-9, 1-58131-897-9, 0-7803-6315-9 (casebound), 0-7803-6316-7 (microfiche). LCCN ???? URL http://delivery.acm.org/10.1145/340000/337428/p316-grun.pdf. IEEE catalog number 00CH37106. ACM order number 477000.

Geary:2006:KGC

[Gea06] Steve Geary. Keynote—Gelato: A call to arms. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/; http://www.ice.gelato.org/about/oct06_presentations.php`.

Gschwind:2000:BTA

[GEAS00] Michael Gschwind, Kemal Ebcioğlu, Erik Altman, and Sumedh Sathaye. Binary translation and architecture convergence issues for IBM System/390. In *Conference proceedings of the 2000 International Conference on Supercomputing: Santa Fe, New Mexico, May 8–11, 2000 [ICS '00]*, pages 336–347. ACM Press, New York, NY, USA, 2000. ISBN 1-58113-270-0. LCCN ???? URL `http://delivery.acm.org/10.1145/340000/335264/p336-gschwind.pdf`.

George:2006:PMI

[Geo06] Jini Susan George. Performance monitoring on Itanium: the PMU counter advantage. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_caliper_george_hp.pdf`.

Geppert:2000:DCT

[Gep00] L. Geppert. Devices and circuits [technology 2000 analysis and forecast]. *IEEE Spectrum*, 37(1):63–69, January 2000. CODEN IEESAM. ISSN 0018-9235 (print), 1939-9340 (electronic).

Geppert:2001:SIP

[Gep01] Linda Geppert. Semiconductors: The Itanium platform lands its first computing systems. *IEEE Spectrum*, 38(7):28–29, July 2001. CODEN IEESAM. ISSN 0018-9235 (print), 1939-9340 (electronic). URL `http://sphinx4.ieee.org/spectrum/jul01/departments/nitan.html; http://sphinx4.ieee.org/spectrum/jul01/pdfs/departments/news0701.pdf`.

Greer:2001:SCI

[GHH+01] Bruce Greer, John Harrison, Greg Henry, Wei Li, and Peter Tang. Scientific computing on the Itanium^{TM} processor. In ACM [ACM01], page ?? ISBN 1-58113-293-X. LCCN ???? URL `http://www.sc2001.org/papers/pap.pap266.pdf`.

Greer:2002:SCI

[GHH+02] Bruce Greer, John Harrison, Greg Henry, et al. Scientific computing on the Itanium(R) processor. *Scientific Programming*, 10(4):329–337, 2002. CODEN SCIPEV. ISSN 1058-9244 (print), 1875-919X (electronic).

Gigante:2006:HPS

[Gig06] Mike Gigante. High-performance storage solutions on IA-64 Linux. In Anonymous [Ano06], page ?? ISBN ???? LCCN

???? URL http://www.ice.gelato.org/; http://www.ice.gelato.org/about/oct06_presentations.php.

Gross:1998:IAP

[GO98] Thomas Gross and David R. O'Hallaron. *iWarp: anatomy of a parallel computing system*. MIT Press, Cambridge, MA, USA, 1998. ISBN 0-262-07183-5. xxiv + 488 pp. LCCN QA76.8.I93 G76 1998.

Gokhale:1996:DOO

[Gok96] Vipin V. Gokhale. Design of the 64-bit option for the Oracle7 relational database management system. *Digital Technical Journal of Digital Equipment Corporation*, 8(4):76–??, ???? 1996. CODEN DTJOEL. ISSN 0898-901X. URL http://www.digital.com:80/info/DTJO06/DTJO06AH.HTM; http://www.digital.com:80/info/DTJO06/DTJO06HM.HTM; http://www.digital.com:80/info/DTJO06/DTJO06P8.PS; http://www.digital.com:80/info/DTJO06/DTJO06PF.PDF; http://www.digital.com:80/info/DTJO06/DTJO06SC.TXT.

Grundy:2000:VOI

[Gru00] Jim Grundy. Verified optimizations for the Intel IA-64 architecture. In Aagaard and Harrison [AH00], pages 215–232. ISBN 3-540-67863-8. LCCN QA267.A1 L43 no.1869; QA76.9.A96 T655 200.

Gwennap:1997:IMI

[Gwe97] Linley Gwennap. *Intel's Merced and IA-64 technology and market forecast*. MicroDesign Resources, Sebastopol, CA, USA, 1997. ISBN 1-885330-13-8. xiv + 96 pp. LCCN QA76.5 .G9524 1997.

Gwennap:1999:IPI

[Gwe99a] Linley Gwennap. IA-64: a parallel instruction set. *Microprocessor Report*, 13(7):1, 6–11, May 31, 1999. ISSN 0899-9341. URL http://www.cs.cmu.edu/afs/cs.cmu.edu/academic/class/15740-f00/public/doc/discussions/uniprocessors/ia64/mpr_ia64_isa_may99.ps.gz.

Gwennap:1999:IDN

[Gwe99b] Linley Gwennap. Intel discloses new IA-64 features. *Microprocessor Report*, 13(3):16–19, March 8, 1999. ISSN 0899-9341. URL http://www.cs.cmu.edu/afs/cs.cmu.edu/academic/class/15740-f00/public/doc/discussions/uniprocessors/ia64/mpr_ia64_regs_mar99.ps.gz.

Gwennap:1999:MSI

[Gwe99c] Linley Gwennap. Merced shows innovative design: Static, dynamic elements work in synergy with compiler. *Microprocessor Report*, 13(13):1, 6–10, October 6, 1999. ISSN 0899-9341.

Gwennap:2000:III

[Gwe00a] Linley Gwennap. *Intel's Itanium and IA-64: technology and market forecast*. MicroDesign Resources, Sunnyvale, CA, USA, 2000. ISBN 1-885330-21-9. iii + 132 pp. LCCN QA76.8.I83 G84 2000.

Gwennap:2000:LLI

[Gwe00b] Linley Gwennap. Linley on Linux: Intel's Itanium on launch pad. *Linux Journal*, 74:62–63, June 2000. CODEN LIJOFX. ISSN 1075-3583 (print), 1938-3827 (electronic). URL `http://noframes.linuxjournal.com/lj-issues/issue74/4019.html`.

Haavind:1997:PIP

[Haa97] Bob Haavind. Peek at IA-64, plus work-a-day embedded processors bow — first details of Intel/H-P explicitly-parallel processor revealed at Microprocessor Forum. *Computer Design*, 36 (12):64–69, ???? 1997. CODEN CMPDAM. ISSN 0010-4566.

Halfhill:1998:II

[Hal98] Tom R. Halfhill. Inside IA-64. *Byte Magazine*, 23(6):81–88, June 1998. CODEN BYTEDJ. ISSN 0360-5280 (print), 1082-7838 (electronic).

Harrison:2000:FVI

[Har00] John Harrison. Formal verification of IA-64 division algorithms. In Aagaard and Harrison [AH00], pages 233–251. ISBN 3-540-67863-8. LCCN QA267.A1 L43 no.1869; QA76.9.A96 T655 200.

Harrison:2003:FVS

[Har03] John Harrison. Formal verification of square root algorithms. *Formal Methods in System Design*, 22(2):143–153, March 2003. CODEN FMSDE6. ISSN 0925-9856 (print), 1572-8102 (electronic). URL `https://dl.acm.org/doi/abs/10.1023/A:1022973506233`.

Hoflehner:2007:CCS

[HDL+07] Gerolf F. Hoflehner, Darshan Desai, Daniel M. Lavery, Alexandru Nicolau, and Alexander V. Veidenbaum. Comparative characterization of SPEC CPU2000 and CPU2006 on Itanium(R) architecture. *ACM SIGMETRICS Performance Evaluation Review*, 35 (1):361–362, June 2007. CODEN ???? ISSN 0163-5999 (print), 1557-9484 (electronic).

HP:2000:IAD

[Hew00a] Hewlett–Packard Corporation, Rockville, MD 20850, USA. *IA-64 Architecture Disclosures*, 2000. ?? pp. URL `http://www.ia64.hp.com/infolibrary/whitepapers/ia64_arch_wp.pdf`.

HP:2000:OIA

[Hew00b] Hewlett–Packard Corporation, Rockville, MD 20850, USA. *Overview of IA-64 Architecture*, 2000. 10 pp. URL `http://devresource.hp.com/STK/partner/ia64bkgnd.pdf`.

This document is part of the HP-UX 11.x Software Transition Kit.

HP:2001:HFV

[Hew01] Hewlett–Packard Company, Palo Alto, CA, USA. *HP Fortran v2.5 for the Itanium Processor Family Release Note*, 2001. 22 pp. URL `http://docs.hp.com/en/5969-7863/5969-7863.pdf`. Manufacturing Part Number: 5969-7863 0601.

Higginbotham:1986:AF

[Hig86] T. F. Higginbotham. Another factor of $(10^{31} - 1)/9$. *ACM SIGNUM Newsletter*, 21(3):12, July 1986. CODEN SNEWD6. ISSN 0163-5778 (print), 1558-0237 (electronic).

Henry:2000:CWW

[HKLS00] Dana S. Henry, Bradley C. Kuszmaul, Gabriel H. Loh, and Rahul Sami. Circuits for wide-window superscalar processors. *ACM SIGARCH Computer Architecture News*, 28(2): 236–247, ???? 2000. CODEN CANED2. ISBN 1-58113-232-8. ISSN 0163-5964 (print), 1943-5851 (electronic). URL `http://delivery.acm.org/10.1145/340000/339689/p236-henry.pdf`. Proceedings of the 27th Annual International Symposium on Computer Architecture: June 12–14, 2000, Vancouver, British Columbia. ACM order number 415004. IEEE catalog number RS00201.

Harrison:2000:HOM

[HKN+00] John Harrison, Ted Kubaska, Bob Norin, Shane Story, and Ping Tak Peter Tang. Highly optimized mathematical functions for the IA-64 architectures. Technical report 245410-002, Intel Corporation, April 2000. URL `ftp://download.intel.com/design/IA-64/Downloads/libm.pdf`.

Hoflehner:2004:COT

[HKS+04] Gerolf Hoflehner, Knud Kirkegaard, Rod Skinner, Daniel Lavery, Yong fong Lee, and Wei Li. Compiler optimizations for transaction processing workloads on Itanium Linux systems. In IEEE [IEE04], pages 294–303. ISBN 0-7695-2126-6. ISSN 1072-4451. LCCN QA76.9.A73. IEEE Computer Society Order Number P2126. ACM Order Number 520040.

Harrison:1999:CTF

[HKST99] John Harrison, Ted Kubaska, Shane Story, and Ping Tak Peter Tang. The computation of transcendental functions on the IA-64 architecture. *Intel Technology Journal*, (Q4):7, November 22, 1999. URL `http://developer.intel.com/technology/itj/q41999/articles/art_5.htm`; `http://developer.intel.com/technology/itj/q41999/pdf/transendental.pdf`.

Huck:2000:IIA

[HMR+00] Jerry Huck, Dale Morris, Jonathan Ross, Allan Knies,

Hans Mulder, and Rumi Zahir. Introducing the IA-64 architecture. *IEEE Micro*, 20(5):12–23, September/October 2000. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL `http://dlib.computer.org/mi/books/mi2000/pdf/m5012.pdf`; `http://www.computer.org/micro/mi2000/m5012abs.htm`.

Hudson:2001:CRG

[HMSW01] Richard L. Hudson, J. Eliot B. Moss, Sreenivas Subramoney, and Weldon Washburn. Cycles to recycle: Garbage collection on the IA-64. *ACM SIGPLAN Notices*, 36(1):101–110, January 2001. CODEN SINODQ. ISBN 1-58113-263-8. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic).

Hammond:2001:NGI

[HN01] Gary Hammond and Sam Naffziger. Next generation Itanium^{TM} processor overview. World-Wide Web slide presentation, August 27–30, 2001. URL `http://cpus.hp.com/technical_references/McK-IDF-2001.pdf`.

Hennessy:2003:CAQ

[HP03a] John L. Hennessy and David A. Patterson. *Computer Architecture—A Quantitative Approach*. Morgan Kaufmann Publishers, San Francisco, CA, USA, third edition, 2003. ISBN 1-55860-596-7. xxi + 883 + A-87 + B-42 + C-1 + D-1 + E-1 + F-1 + G-1 + H-1 + I-1 + R-22 + I-44 pp. LCCN QA76.9.A73 P377 2003. US$89.95. URL `http://www.mkp.com/books_catalog/catalog.asp?ISBN=1-55860-596-7`; `http://www.mkp.com/CA3`.

Hennessy:2003:PIA

[HP03b] John L. Hennessy and David A. Patterson. Putting it all together: The Intel IA-64 architecture and Itanium processor. In *Computer Architecture—A Quantitative Approach* [HP03a], pages 351–362. ISBN 1-55860-596-7. LCCN QA76.9.A73 P377 2003. US$89.95. URL `http://www.mkp.com/books_catalog/catalog.asp?ISBN=1-55860-596-7`; `http://www.mkp.com/CA3`.

Hennessy:2006:III

[HP06] John L. Hennessy and David A. Patterson. The Intel IA-64 and Itanium processor. In *Computer Architecture: A Quantitative Approach* [HPAD$^+$06], pages G–32–G–43. ISBN 0-12-370490-1 (paperback). LCCN QA76.9.A73 P377 2006. URL `http://www.loc.gov/catdir/enhancements/fy0665/2006024358-d.html`; `http://www.loc.gov/catdir/toc/ecip0618/2006024358.html`.

Hennessy:2006:CAQ

[HPAD$^+$06] John L. Hennessy, David A. Patterson, Andrea C. Arpaci-Dusseau, et al. *Computer Architecture: A Quantitative Approach*. Morgan Kauf-

mann Publishers, Boston, MA, USA, fourth edition, 2006. ISBN 0-12-370490-1 (paperback). ???? pp. LCCN QA76.9.A73 P377 2006. URL http://www.loc.gov/catdir/enhancements/fy0665/2006024358-d.html; http://www.loc.gov/catdir/toc/ecip0618/2006024358.html.

Heil:1999:IBP

[HSS99] Timothy H. Heil, Zak Smith, and J. E. Smith. Improving branch predictors by correlating on data values. In *Proceedings: 32nd Annual International Symposium on Microarchitecture: Haifa, Israel, November 16–18, 1999*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 1999. ISBN 0-7695-0437-X. LCCN QA76.6.I5736 1999. URL http://delivery.acm.org/10.1145/330000/320086/p28-heil.pdf. IEEE Computer Society order number PR00437.

Huang:2006:CLK

[Hua06] Feilong Huang. Compiling the Linux kernel with the Intel compiler. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL http://www.ice.gelato.org/; http://www.ice.gelato.org/about/oct06_presentations.php.

Hughes:2000:PJ

[Hug00a] Phil Hughes. From the publisher: January 2000. *Linux Journal*, 69:??, January 2000. CODEN LIJOFX. ISSN 1075-3583 (print), 1938-3827 (electronic).

Hughes:2000:PUL

[Hug00b] Phil Hughes. From the publisher: UnixWare and Linux get hitched. *Linux Journal*, 78: ??, October 2000. CODEN LIJOFX. ISSN 1075-3583 (print), 1938-3827 (electronic).

Hung:2006:HPH

[Hun06] Terence Hung. Host presentation—HPC and Grid R&D activities at IHPC. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_ihpc_hung_ihpc.pdf.

IBM:2000:MCC

[IBM00] IBM. Migrating C and C++ applications to AIX 5L on IA-64. World-Wide Web document., October 3, 2000. URL http://www-1.ibm.com/servers/aix/itanium/devtools/migratingcandc++.pdf.

IEEE:1997:HCI

[IEE97] IEEE, editor. *Hot Chips IX: Stanford University, Stanford, California, August 24–26, 1997*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 1997. ISBN ???? LCCN ????

IEEE:1999:HCS

[IEE99] IEEE, editor. *Hot Chips 11: Stanford University, Stanford,*

California, August 15–17, 1999. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 1999. ISBN ???? LCCN ???? URL `http://www.hotchips.org/hotc11_index.html`.

IEEE:2000:HCS

[IEE00] IEEE, editor. *Hot Chips 12: Stanford University, Stanford, California, August 13–15, 2000*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2000. ISBN ???? LCCN ???? URL `http://www.hotchips.org/index12.html`.

IEEE:2002:IIS

[IEE02] IEEE, editor. *IEEE International Solid-State Circuits Conference (ISSCC 2002), February 4–6, 2002, San Francisco Marriott Hotel, San Francisco, CA, USA*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2002. ISBN ???? ISSN 0743-1686. LCCN ???? URL `http://www.sscs.org/isscc/`.

IEEE:2003:PCI

[IEE03] IEEE, editor. *Proceedings of the 2003 CGO: the International Symposium on Code Generation and Optimization; March 23–26, 2003, Fisherman's Wharf, San Francisco, CA, with special emphasis on feedback-directed and runtime optimization*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2003. ISBN 0-7695-1913-X. LCCN ???? ACM Order No. 530033.

IEEE:2004:PIS

[IEE04] IEEE, editor. *Proceedings: 37th International Symposium on Microarchitecture, MICRO-37: 4–8 December 2004, Portland, Oregon*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2004. ISBN 0-7695-2126-6. ISSN 1072-4451. LCCN QA76.9.A73. IEEE Computer Society Order Number P2126. ACM Order Number 520040.

IEEE:2005:PIS

[IEE05] IEEE, editor. *Proceedings of the 17th IEEE Symposium on Computer Arithmetic, ARITH-17, June 27–29, 2005, Cape Cod, Massachusetts, USA*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2005. ISBN ???? LCCN ????

Inagaki:2003:IPS

[IKN03] Tatsushi Inagaki, Hideaki Komatsu, and Toshio Nakatani. Integrated prepass scheduling for a Java Just-In-Time compiler on the IA-64 architecture. In IEEE [IEE03], pages 159–168. ISBN 0-7695-1913-X. LCCN ???? ACM Order No. 530033.

Intel:1999:IAD

[Int99] Intel Corporation. *IA-64 Application Developer's Architecture Guide*. Intel Corporation, Santa Clara, CA, USA, May

1999. ISBN ???? 476 pp. LCCN ???? URL http://developer.intel.com/design/ia-64/downloads/ADAG.pdf.

Intel:2000:AIC

[Int00a] Intel Corporation. The advantages of IA-64 for cache server software information for software developers and IT managers. Technical report, Intel Corporation, Santa Clara, CA, USA, 2000. 5 pp. URL http://developer.intel.com/design/ia-64/downloads/ia-64_cache2.htm.

Intel:2000:DIG

[Int00b] Intel Corporation. Developer's interface guide for IA-64 servers. Technical report, Intel Corporation, Santa Clara, CA, USA, 2000. URL http://developer.intel.com/design/servers/dev_guides/content/doc_lib/index.htm. This document is a directory of pointers to white papers on the DIG-64 (Developer's Interface Guide) specifications.

Intel:2000:ISAa

[Int00c] Intel Corporation. *IA-64 System Abstraction Layer (SAL) Specification*. Intel Corporation, Santa Clara, CA, USA, July 2000. ISBN ???? 120 pp. LCCN ???? URL http://developer.intel.com/design/ia-64/downloads/24535902.htm.

Intel:2000:ISAb

[Int00d] Intel Corporation. The IA-64 system architecture: Tutorial for hardware, OS, and application developers. Technical report, Intel Corporation, Santa Clara, CA, USA, 2000. URL http://developer.intel.com/design/ia-64/archSysSoftware/.

Intel:2000:IIAa

[Int00e] Intel Corporation. *Intel IA-64 Architecture Software Developer's Manual: Volume 1: IA-64 Application Architecture*. Intel Corporation, Santa Clara, CA, USA, January 2000. ISBN ???? 216 pp. LCCN ???? URL http://developer.intel.com/design/ia-64/downloads/245317.htm.

Intel:2000:IIAb

[Int00f] Intel Corporation. *Intel IA-64 Architecture Software Developer's Manual: Volume 2: IA-64 System Architecture*. Intel Corporation, Santa Clara, CA, USA, January 2000. ISBN ???? 536 pp. LCCN ???? URL http://developer.intel.com/design/ia-64/downloads/245318.htm.

Intel:2000:IIAc

[Int00g] Intel Corporation. *Intel IA-64 Architecture Software Developer's Manual: Volume 3: Instruction Set Reference*. Intel Corporation, Santa Clara, CA, USA, January 2000. ISBN ???? 926 pp. LCCN ???? URL http://developer.intel.com/design/ia-64/downloads/245319.htm.

Intel:2000:IIAd

[Int00h] Intel Corporation. *Intel IA-64 Architecture Software Developer's Manual: Volume 4: Itanium Processor Programmer's Guide*. Intel Corporation, Santa Clara, CA, USA, January 2000. ISBN ???? 76 pp. LCCN ???? URL http://developer.intel.com/design/ia-64/downloads/245320.htm.

Intel:2000:IIP

[Int00i] Intel Corporation. Intel Itanium processor: High performance on security algorithms (RSA decryption kernel). Technical report, Intel Corporation, Santa Clara, CA, USA, 2000. 8 pp. URL http://developer.intel.com/design/ia-64/downloads/itaniumssl_seg_103.htm.

Intel:2000:IBL

[Int00j] Intel Corporation. *Itanium-Based Linux Developer's Kit*. Intel Corporation, Santa Clara, CA, USA, 2000. ISBN ???? ???? pp. LCCN ???? URL http://developer.intel.com/design/ia-64/linux.htm.

Intel:2000:IPF

[Int00k] Intel Corporation, Santa Clara, CA, USA. *Itanium Processor Floating-point Software Assistance and Floating-point Exception Handling*, January 2000. URL http://cache-www.intel.com/cd/00/00/21/92/219290_fpswa_software.pdf.

Intel:2000:IPMa

[Int00l] Intel Corporation. *Itanium Processor Microarchitecture Reference for Software Optimization*. Intel Corporation, Santa Clara, CA, USA, March 2000. ISBN ???? 32 pp. LCCN ???? URL http://developer.intel.com/design/ia-64/downloads/245473.htm.

Intel:2000:IPMb

[Int00m] Intel Corporation. *Itanium Processor Microarchitecture Reference for Software Optimization*. Intel Corporation, Santa Clara, CA, USA, August 2000. ISBN ???? 34 pp. LCCN ???? URL http://developer.intel.com/design/ia-64/downloads/245474.htm.

Doshi:2000:IPP

[Int00n] Intel Corporation. Itanium processor program update. Technical report, Intel Corporation, Santa Clara, CA, USA, 2000. URL http://developer.intel.com/design/ia-64/IDFprogram_progress/.

Intel:2003:DSR

[Int03a] Intel. Divide, square root, and remainder algorithms for the Itanium architecture. Intel Software Development Products, December 18, 2003. URL http://www.intel.com/cd/software/products/asmona/eng/219863.htm.

Intel:2003:NID

[Int03b] Intel. Non-IEEE division, square root, reciprocal, and reciprocal square root algorithms for the Intel Itanium architecture. Intel Software Development Products, December 18, 2003. URL `http://www.intel.com/cd/software/products/asmo-na/eng/219864.htm`.

Jarp:1999:IAD

[Jar99] Sverre Jarp. IA-64 architecture: A detailed tutorial. World-Wide Web slide presentation, November 1999. URL `http://sverre.home.cern.ch/sverre/IA64_1.pdf`.

Jarp:2001:OIP

[Jar01] Sverre Jarp. Optimizing IA-64 performance. *Dr. Dobb's Journal of Software Tools*, 26(7):21–22, 24, 26, July 2001. CODEN DDJOEB. ISSN 1044-789X. URL `http://www.ddj.com/ftp/2001/2001_07/ia64.txt; http://www.ddj.com/ftp/2001/2001_07/ia64.zip`.

Johnson:2002:OIB

[JM02] Teresa Johnson and Nathaniel McIntosh. Optimizing Itanium-based applications. Technical report, Hewlett–Packard Corporation, Palo Alto, CA, USA, 2002. URL `http://h21007.www2.hp.com/dspp/tech/tech_TechDocumentDetailPage_IDX/1,1701,3207,00.html`. Version 1.3.

Johnson:2006:SLO

[Joh06a] Doug Johnson. Storage layout optimizations to improve parallel distributed filesystem performance. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/; http://www.ice.gelato.org/about/oct06_presentations.php`.

Johnsson:2006:EIC

[Joh06b] Lennart Johnsson. Experiences with Itanium clusters in Grids. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_clustergrid_johnsson_uhouston.pdf`.

Josephson:2002:DMM

[JPG02] Don Douglas Josephson, Steve Poehlman, and Vincent Govan. Debug methodology for the McKinley processor. In IEEE [IEE02], pages 451–460. ISBN ???? ISSN 0743-1686. LCCN ???? URL `http://cpus.hp.com/technical_references/itc_2001/debug_paper.pdf`.

Josephson:2002:TMMa

[JPGM02a] Doug Josephson, Steve Poehlman, Vincent Govan, and Clint Mumford. Test methodology for the McKinley processor. In IEEE [IEE02], pages 578–585. ISBN ???? ISSN 0743-1686. LCCN ???? URL `http://cpus.hp.com/technical_references/itc_2001/test_paper.pdf`.

Josephson:2002:TMMb

[JPGM02b] Doug Josephson, Steve Poehlman, Vincent Govan, and Clint Mumford. Test methodology for the McKinley processor. World-Wide Web slide presentation, 2002. URL `http://cpus.hp.com/technical_references/itc_2001/test_slides.pdf`.

Jacobowitz:1998:LE

[JR98] Norman M. Jacobowitz and Eric S. Raymond. Linux Expo 1998. *Linux Journal*, 52:??, August 1998. CODEN LIJOFX. ISSN 1075-3583 (print), 1938-3827 (electronic).

Jurga:2006:PEP

[Jur06] Ryszard Erazm Jurga. Practical experience with performance monitors on Xeon and Itanium. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_pmuexperience_jurga_cern.pdf`.

Konagaya:2006:PSS

[KA06] Akihiko Konagaya and Ryuzo Azuma. Particle simulation for subcellular dynamics and localization of biological molecules. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_partsim_konagaya_riken.pdf`.

Karger:2007:PSL

[Kar07] Paul A. Karger. Performance and security lessons learned from virtualizing the Alpha processor. *ACM SIGARCH Computer Architecture News*, 35(2): 392–401, May 2007. CODEN CANED2. ISSN 0163-5964 (print), 1943-5851 (electronic).

Kennedy:1997:NPC

[KBC+97] Ken Kennedy, Charles F. Bender, John W. D. Connolly, John L. Hennessy, Mary K. Vernon, and Larry Smarr. A nationwide parallel computing environment. *Communications of the ACM*, 40(11): 62–72, November 1997. CODEN CACMA2. ISSN 0001-0782 (print), 1557-7317 (electronic). URL `http://www.acm.org:80/pubs/citations/journals/cacm/1997-40-11/p62-kennedy/`.

Knies:1999:TIA

[KFL99] Allan Knies, Jesse Fang, and Wei Li. Tutorial: IA64 architecture and compilers. In IEEE [IEE99], page ?? ISBN ???? LCCN ???? URL `http://www.hotchips.org/hotc11_index.html`.

Kondo:2001:OIS

[KI01] T. Kondo and Y. Ito. Overview of Itanium 16way server "AzusA". *NEC Technical Journal = NEC giho*, 54(10):13–14, 2001. CODEN NECGEZ. ISSN 0285-4139.

Koren:1999:ISC

[KK99] Israel Koren and Peter Kornerup, editors. *14th IEEE Symposium on Computer Arithmetic: proceedings: April 14–16, 1999, Adelaide, Australia*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 1999. ISBN 0-7803-5609-8, 0-7695-0116-8, 0-7695-0118-4. ISSN 1063-6889. LCCN QA76.6 .S887 1999. URL `http://computer.org/conferen/home/arith/; http://www.ecs.umass.edu/ece/arith14/program.html`. IEEE Computer Society Order Number PR00116. IEEE Order Plan Catalog Number 99CB36336.

Kennai:2001:WAI

[KKH+01] E. Kennai, H. Kawashima, Hagiwara, Y., et al. Windows OS and applications for Itanium. *NEC Technical Journal = NEC giho*, 54(10):48–51, 2001. CODEN NECGEZ. ISSN 0285-4139.

Krishnaiyer:2000:AOI

[KKL+00] Rakesh Krishnaiyer, Dattatraya Kulkarni, Daniel Lavery, Wei Li, Chu cheow Lim, John Ng, and David Sehr. An advanced optimizer for the IA-64 architecture. *IEEE Micro*, 20(6):60–68, November/December 2000. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL `http://dlib.computer.org/mi/books/mi2000/pdf/m6060.pdf; http://www.computer.org/micro/mi2000/m6060abs.htm`.

Kawahito:2006:ESE

[KKN06] Motohiro Kawahito, Hideaki Komatsu, and Toshio Nakatani. Effective sign extension elimination for Java. *ACM Transactions on Programming Languages and Systems*, 28(1):106–133, January 2006. CODEN ATPSDT. ISSN 0164-0925 (print), 1558-4593 (electronic).

Kimura:2001:MSI

[KNH+01] K. Kimura, K. Naitoh, K. Hirata, et al. Middle software on Itanium. *NEC Technical Journal = NEC giho*, 54(10):56–59, 2001. CODEN NECGEZ. ISSN 0285-4139.

Knies:1999:IAB

[Kni99a] Allan Knies. IA-64 architecture basics/introduction. In IEEE [IEE99], page ?? ISBN ???? LCCN ???? URL `http://www.hotchips.org/hotc11_index.html`.

Knies:1999:OTU

[Kni99b] Allan Knies. Optimization techniques/using IA-64 features. In IEEE [IEE99], page ?? ISBN ???? LCCN ???? URL `http://www.hotchips.org/hotc11_index.html`.

Kobayashi:2001:RSI

[Kob01] K. Kobayashi. Remarks for special issue on Itanium-based server and workstation products. *NEC Technical Journal = NEC giho*, 54(10):1–2, 2001.

CODEN NECGEZ. ISSN 0285-4139.

Krause:1998:UM

[Kra98] Jason Krause. Unixes for Merced. *Byte Magazine*, 23 (5):25–26, May 1998. CODEN BYTEDJ. ISSN 0360-5280 (print), 1082-7838 (electronic).

Kreinovich:2001:INB

[Kre01a] Vladik Kreinovich. Itanium's new basic operation of fused multiply-add: Theoretical explanation and theoretical challenge. *ACM SIGACT News*, 32 (1):115–117, 2001. URL `http://www.cs.utep.edu/vladik/2000/tr00-42.pdf; http://www.cs.utep.edu/vladik/2000/tr00-42.ps.gz`.

Krewell:2001:IRI

[Kre01b] Kevin Krewell. Intel raises the Itanium: First IA-64 processor released at 733MHz and 800MHz. *Microprocessor Report*, ??(??):??, June 11, 2001. ISSN 0899-9341. URL `http://www.mdronline.com/mpr/h/2001/0611/152401.html`.

Kroll:1999:VLW

[Kro99] Jason Kroll. VA Linux workstation VArStation XMP. *Linux Journal*, 67:??, November 1999. CODEN LIJOFX. ISSN 1075-3583 (print), 1938-3827 (electronic). URL `http://noframes.linuxjournal.com/lj-issues/issue67/3653.html`.

Kroll:2000:RCA

[Kro00a] Jason Kroll. 1999 readers' choice awards: You voted, we counted — here are the results. *Linux Journal*, 69:??, January 2000. CODEN LIJOFX. ISSN 1075-3583 (print), 1938-3827 (electronic).

Kroll:2000:NOS

[Kro00b] Jason Kroll. Netwinder office server. *Linux Journal*, 72:??, April 2000. CODEN LIJOFX. ISSN 1075-3583 (print), 1938-3827 (electronic).

Kulkarni:2006:SCS

[Kul06] Pankaj Kulkarni. S7 case study: Porting 2 million lines of C++ code to HP-UX Itanium. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_s7study_kulkarni_s7softwaresolutions.pdf`.

Kraemer:2001:SCV

[KvG01] W. Krämer and Jürgen Wolff von Gudenberg, editors. *Scientific Computing, Validated Numerics, Interval Methods*. Kluwer Academic Publishers Group, Norwell, MA, USA, and Dordrecht, The Netherlands, 2001. ISBN 0-306-46706-2. LCCN ???? 09.00 EUR / 95.00 USD / 66.50 GBP. URL `http://www.wkap.nl/prod/b/0-306-46706-2`. Scan 2000, the GAMM–IMACS International Symposium on Scientific Computing, Computer Arithmetic,

and Validated Numerics and Interval 2000, the International Conference on Interval Methods in Science and Engineering were jointly held in Karlsruhe, September 19–22, 2000.

Kastner:2001:IBI

[KW01] Daniel Kästner and Sebastian Winkel. ILP-based instruction scheduling for IA-64. *ACM SIGPLAN Notices*, 36(8):145–154, August 2001. CODEN SINODQ. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic).

Lau:2006:IPR

[Lau06] Jon Lau. Itanium projects: From R&D to industry. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_projects_lau_ngo.pdf`.

Larin:1999:CDC

[LC99] S. Y. Larin and T. M. Conte. Compiler-driven cached code compression schemes for embedded ILP processors. In *Proceedings: 32nd Annual International Symposium on Microarchitecture: Haifa, Israel, November 16–18, 1999*, pages 82–92. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 1999. ISBN 0-7695-0437-X. LCCN QA76.6.I5736 1999. URL `http://ieeexplore.ieee.org/iel5/6577/17552/00809446.pdf`.

Lin:2003:SRP

[LCHY03] Jin Lin, Tong Chen, Wei-Chung Hsu, and Pen-Chung Yew. Speculative register promotion using advanced load address table (ALAT). In IEEE [IEE03], pages 125–134. ISBN 0-7695-1913-X. LCCN ???? ACM Order No. 530033.

Lee:2006:HPN

[Lee06] Hing Yan Lee. Host presentation—National Grid Office in Singapore. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_ngo_lee_ngo.pdf`.

Lehrbaum:2000:ESNa

[Leh00a] Rick Lehrbaum. Embedded systems news briefs. *Linux Journal*, 71:??, March 2000. CODEN LIJOFX. ISSN 1075-3583 (print), 1938-3827 (electronic).

Lehrbaum:2000:ESNc

[Leh00b] Rick Lehrbaum. Embedded systems news briefs. *Linux Journal*, 73:??, May 2000. CODEN LIJOFX. ISSN 1075-3583 (print), 1938-3827 (electronic).

Lewis:1999:BCFb

[Lew99] Ted Lewis. Binary critic: Fast, expensive, and horribly complex. *Computer*, 32 (9):120, 118–119, September 1999. CODEN CPTRB4. ISSN 0018-9162 (print), 1558-0814 (electronic). URL `http://developer.intel.com/design/`

ia64/index.htm; http://dlib.computer.org/co/books/co1999/pdf/r9120.pdf.

Li:2001:CIA

[Li01] Wei Li. Compiling for Itanium architecture: Triumphs and challenges. Technical report, Hewlett–Packard Corporation, Palo Alto, CA, USA, 2001. URL http://systems.cs.colorado.edu/EPIC1/.

Liu:2006:UOP

[Liu06] Shin-Ming Liu. Update on the Osprey Project, the alternative GCC backend for Itanium. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_osprey_liu_hp.pdf.

Launchbury:1999:EMD

[LLC99] John Launchbury, Jeffrey R. Lewis, and Byron Cook. On embedding a microarchitectural design language within Haskell. In *Proceedings of the ACM SIGPLAN international conference on functional programming (ICFP '99), Paris, France, September 27–29, 1999*, volume 34(9) of *ACM SIGPLAN Notices*, pages 60–69. ACM Press, New York, NY, USA, September 1999. ISBN 1-58113-111-9. LCCN QA76.7 .A1095 v.34 no.9 1999. URL http://delivery.acm.org/10.1145/320000/317784/p60-launchbury.pdf.

Li:2001:LLF

[LMOT01] Ren-Cang Li, Peter Markstein, Jon P. Okada, and James W. Thomas. The libm library and floating-point arithmetic for HP-UX on Itanium. Technical report, Hewlett–Packard Corporation, Palo Alto, CA, USA, April 2001. ?? pp. URL http://h21007.www2.hp.com/dspp/ddl/ddl_Download_File_TRX/1,1249,942,00.pdf; http://h21007.www2.hp.com/dspp/tech/tech_TechDocumentDetailPage_IDX/1,1701,981,00.html.

Li:2002:LLF

[LMOT02] Ren-Cang Li, Peter Markstein, Jon P. Okada, and James W. Thomas. The libm library and floating-point arithmetic for HP-UX on Itanium-2. Technical report, Hewlett–Packard Corporation, Palo Alto, CA, USA, 2002. ?? pp. URL ????.

Lucco:2000:SSD

[Luc00] Steven Lucco. Split-stream dictionary program compression. *ACM SIGPLAN Notices*, 35(5):27–34, May 2000. CODEN SINODQ. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic). URL http://delivery.acm.org/10.1145/350000/349307/p27-lucco.pdf; http://www.acm.org/pubs/articles/proceedings/pldi/349299/p27-lucco/p27-lucco.pdf; http://www.acm.org/pubs/citations/proceedings/pldi/349299/p27-lucco/.

Markstein:2000:IEF

[Mar00] Peter Markstein. *IA-64 and Elementary Functions: Speed and Precision*. Hewlett–Packard professional books. Prentice-Hall, Upper Saddle River, NJ 07458, USA, 2000. ISBN 0-13-018348-2. xix + 298 pp. LCCN QA76.9.A73 M365 2000. URL `http://www.markstein.org/`.

Markstein:2003:FQP

[Mar03a] Peter Markstein. A fast quad precision elementary function library for Itanium. In Anonymous [Ano03], pages 5–12. ISBN ???? LCCN ????

Martin:2003:ERG

[Mär03b] Christian Märtin. *Einführung in die Rechnerarchitektur. (German) [Introduction to Computer Architecture]*. Carl Hanser, München, Germany, 2003. ISBN 3-446-22242-1. 170 pp. LCCN ???? 14,90 Eur[D]; 15,40 Eur[A]; 23,30 sFr. Includes CD-ROM.

Markstein:2005:FSM

[Mar05] Peter Markstein. A fast-start method for computing the inverse tangent. In IEEE [IEE05], page ?? ISBN ???? LCCN ???? URL `http://arith17.polito.it/final/paper-112.pdf`.

Vachharajani:2004:FPF

[Mat04] Manish Vachharajani. Matthew Iyer, Chinmay Ashok, Josh Stone, Neil Vachharajani, Daniel A. Connors. Finding parallelism for future EPIC machines. In ????, editor, *Proceedings of the 4th Workshop on Explicitly Parallel Instruction Computing. March, 2005.*, page ?? ????, ????, 2004. ISBN ???? LCCN ???? URL `http://rogue.colorado.edu/draco/abstract.php?pub=epic05-ilp.pub&paper_dir=papers; http://rogue.colorado.edu/draco/papers/epic05-ilp.pdf; http://rogue.colorado.edu/draco/papers/epic05-ilp.ps`.

McNairy:2005:MDC

[MB05] Cameron McNairy and Rohit Bhatia. Montecito: A dual-core, dual-thread Itanium processor. *IEEE Micro*, 25 (2):10–20, March/April 2005. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL `http://csdl.computer.org/comp/mags/mi/2005/02/m2010abs.htm; http://csdl.computer.org/dl/mags/mi/2005/02/m2010.pdf`.

Mouli:2007:FF

[MC07] C. Mouli and W. Carriker. Future fab. *IEEE Spectrum*, 44 (3):38–43, March 2007. CODEN IEESAM. ISSN 0018-9235 (print), 1939-9340 (electronic).

McNairy:2006:BII

[McN06a] Cameron McNairy. Basic Intel Itanium architecture. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/; http://`

www.ice.gelato.org/about/oct06_presentations.php.

McNairy:2006:HTD

[McN06b] Cameron McNairy. Hyper-threading on dual-core Intel Itanium 2 processors. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL http://www.ice.gelato.org/; http://www.ice.gelato.org/about/oct06_presentations.php.

Mosberger:2002:ILK

[ME02] David Mosberger and Stéphane Eranian. *IA-64 Linux kernel: design and implementation*. Hewlett–Packard professional books. Prentice-Hall PTR, Upper Saddle River, NJ 07458, USA, 2002. ISBN 0-13-061014-3. 559 (est.) pp. LCCN QA76.9.A73 M67 2002. US$59.99.

Mackin:2007:MSP

[MHTH07] J. C. Mackin, Mike Hotek, Tobias Thernström, and Shannon Horn. *MCITP self-paced training kit (Exam 70-443): designing a database server infrastructure using Microsoft SQL Server 2005*. Microsoft Press, Bellevue, WA, USA, 2007. ISBN 0-7356-2173-X. xxxii + 708 pp. LCCN QA76.3 .M3224 2007. URL http://www.loc.gov/catdir/toc/fy0711/2006932079.html.

McInerney:2000:MRI

[MLH+00] R. McInerney, K. Leeper, T. Hill, H. Chan, B. Basaran, and L. McQuiddy. Methodology for repeater insertion management in the RTL, layout floorplan and fullchip timing databases of the Itanium microprocessor. In ACM [ACM00], pages 99–104.

Moore:1965:CMC

[Moo65] Gordon E. Moore. Cramming more components onto integrated circuits. *Electronics*, 38 (8):114–117, 1965. URL http://www.intel.com/technology/mooreslaw/index.htm.

Moore:2006:OSI

[Moo06] Eric W. Moore. Optimizing software for Intel Itanium architecture with Intel compilers. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL http://www.ice.gelato.org/; http://www.ice.gelato.org/about/oct06_presentations.php.

Manson:2001:CSM

[MP01] Jeremy Manson and William Pugh. Core semantics of multithreaded Java. In *ISCOPE Conference on ACM 2001 Java Grande*, pages 29–38. ACM Press, New York, NY, USA, 2001. CODEN NECGEZ. ISBN 1-58113-359-6. ISSN 0285-4139. LCCN ???? URL http://delivery.acm.org/10.1145/380000/376806/p29-manson.pdf.

McNairy:2003:IPM

[MS03] Cameron McNairy and Don

Soltis. Itanium 2 processor microarchitecture. *IEEE Micro*, 23(2):44–55, March/April 2003. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL http://dlib.computer.org/mi/books/mi2003/pdf/m2044.pdf; http://www.computer.org/micro/mi2003/m2044abs.htm.

Mikayama:2001:ISR

[MSN+01] S. Mikayama, I. Sugasaki, Y. Nishikawa, et al. Itanium 16way server RAS firmware. *NEC Technical Journal = NEC giho*, 54(10):29–32, 2001. CODEN NECGEZ. ISSN 0285-4139.

Machanick:1998:HST

[MSP98] Philip Machanick, Pierre Salverda, and Lance Pompe. Hardware-software trade-offs in a direct Rambus implementation of the RAMpage memory hierarchy. *ACM SIGPLAN Notices*, 33(11):105–114, November 1998. CODEN SINODQ. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic). URL http://delivery.acm.org/10.1145/300000/291032/p105-machanick.pdf; http://www.acm.org:80/pubs/citations/proceedings/asplos/291069/p105-machanick/.

Hwu:1998:RIA

[mWH98] Wen mei W. Hwu. Retrospective: IMPACT: an architectural framework for multiple-instruction issue. In Gurindar Sohi, editor, *25 years of the International Symposia on Computer Architecture (selected papers)*, pages 77–79. ACM Press, New York, NY, USA, 1998. ISBN 1-58113-058-9. LCCN QA76.9.A73 S944 1998. URL http://delivery.acm.org/10.1145/290000/285960/p77-hwu.pdf.

Nance:1998:UGM

[Nan98] Barry Nance. Unix gears up for Merced. SCO's new UnixWare. *Byte Magazine*, 23(5):45, May 1998. CODEN BYTEDJ. ISSN 0360-5280 (print), 1082-7838 (electronic).

Neuner:2006:ILS

[Neu06] Steve Neuner. An inside look at scaling Linux to 1024 processors. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_scaling1024_neuner_sgi.pdf.

Naffziger:2002:ING

[NH02] Samuel D. Naffziger and Gary Hammond. The implementation of the next generation 64b Itanium^{TM} microprocessor. In IEEE [IEE02], page ?? ISBN ???? ISSN 0743-1686. LCCN ???? URL http://cpus.hp.com/technical_references/isscc_2002/isscc_2002_1.shtml; http://www.intel.com/design/Itanium2/techpubs/.

NIST:2000:TAE

[NIS00] NIST, editor. *The Third Advanced Encryption Standard Candidate Conference, April 13–14, 2000, New York, NY, USA*. National Institute for Standards and Technology, Gaithersburg, MD, USA, 2000. ISBN ???? LCCN ???? URL `http://csrc.nist.gov/encryption/aes/round2/conf3/aes3conf.htm; http://csrc.nist.gov/encryption/aes/round2/conf3/papers/AES3Proceedings-1.pdf; http://csrc.nist.gov/encryption/aes/round2/conf3/papers/AES3Proceedings-2.pdf; http://csrc.nist.gov/encryption/aes/round2/conf3/papers/AES3Proceedings-3.pdf; http://csrc.nist.gov/encryption/aes/round2/conf3/papers/AES3Proceedings.pdf`.

Nishioka:2001:AOS

[NTN+01] H. Nishioka, Y. Taya, M. Nishikayama, et al. Automatic operation system of Itanium 16way server. *NEC Technical Journal = NEC giho*, 54(10):33–36, 2001. CODEN NECGEZ. ISSN 0285-4139.

Paul:2001:IIC

[Pau01] L. G. Paul. Intel's Itanium chip positions new workstations to rival Unix machines. *Managing automation*, 16(9):50–55, 2001. CODEN NECGEZ. ISSN 0285-4139.

Pinsky:2006:GCC

[Pin06] Lawrence Pinsky. Grid computing at CERN: An update on preparations for first beam in 2007. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_gridlhc_pinsky_uhouston.pdf`.

Poniatowski:2005:LHI

[Pon05] Marty Poniatowski. *Linux on HP Integrity Servers: system administration for Itanium-based systems*. Prentice-Hall PTR, Upper Saddle River, NJ 07458, USA, 2005. ISBN 0-13-140000-2. xxvi + 332 pp. LCCN QA76.76.O63 P652 2005.

Popovich:2002:ILN

[Pop02] Ken Popovich. Intel looks to next Itanium: 64-bit processor and hyperthreading for Xeon chips will star at Intel's developer conference. *eWeek*, 19(8): 16, February 25, 2002. CODEN ???? ISSN 1530-6283.

Partel:2001:DHU

[POY+01] M. Partel, D. Olander, M. Yoder, et al. Development of HP-UX for Itanium processor family. *NEC Technical Journal = NEC giho*, 54(10):44–47, 2001. CODEN NECGEZ. ISSN 0285-4139.

Pranevich:1998:KKW

[Pra98] Joseph Pranevich. Kernel korner: The wonderful world of

Linux 2.2. *Linux Journal*, 56:46–49, December 1998. CODEN LIJOFX. ISSN 1075-3583 (print), 1938-3827 (electronic).

Qiu:1998:ODA

[QD98] Xiaogang Qiu and Michel Dubois. Options for dynamic address translation in COMAs. In *Proceedings of the 25th annual international symposium on Computer architecture*, pages 214–225. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 1998. ISSN 0163-5964 (print), 1943-5851 (electronic). URL `http://delivery.acm.org/10.1145/280000/279390/p214-qiu.pdf`.

Quintana-Orti:2009:ULF

[QOV09] Enrique S. Quintana-Ortí and Robert A. Van De Geijn. Updating an LU factorization with pivoting. *ACM Transactions on Mathematical Software*, 35 (2):11:1–11:16, July 2009. CODEN ACMSCU. ISSN 0098-3500 (print), 1557-7295 (electronic).

Quach:2000:HAR

[Qua00a] Nhon Quach. High-availability and reliability in the Itanium processor. *IEEE Micro*, 20(5):61–69, September/October 2000. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL `http://dlib.computer.org/mi/books/mi2000/pdf/m5061.pdf; http://www.computer.org/micro/mi2000/m5061abs.htm`.

Quach:2000:IPF

[Qua00b] Nhon Quach. The Itanium processor features for high availability and reliability. In IEEE [IEE00], page ?? ISBN ???? LCCN ???? URL `http://www.hotchips.org/index12.html`.

Ramakrishna:1993:DST

[Ram93] B. Ramakrishna. Dynamic scheduling techniques for VLIW processors. Technical Report HPL-93-52, Hewlett–Packard Corporation, Palo Alto, CA, USA, 1993. URL `http://www.hpl.hp.com/techreports/`.

Rong:2008:RAS

[RDG08] Hongbo Rong, Alban Douillet, and Guang R. Gao. Register allocation for software pipelined multidimensional loops. *ACM Transactions on Programming Languages and Systems*, 30(4): 23:1–23:??, July 2008. CODEN ATPSDT. ISSN 0164-0925 (print), 1558-4593 (electronic).

Rau:1992:ILP

[RF92] B. Ramakrishna Rau and Joseph A. Fisher. Instruction-level parallel processing: History, overview, and perspective. Technical Report HPL-92-132, Hewlett–Packard Corporation, Palo Alto, CA, USA, 1992. URL `http://www.hpl.hp.com/techreports/`.

Rau:1993:ILP

[RF93] Bantwal Ramakrishna Rau and Joseph A. Fisher, editors. *Instruction-level parallelism: a special issue of The Journal of Supercomputing*, volume SECS 235 of *The Kluwer international series in engineering and computer science*. Kluwer Academic Publishers Group, Norwell, MA, USA, and Dordrecht, The Netherlands, 1993. ISBN 0-7923-9367-8. 282 pp. LCCN QA76.58 .I49 1993.

Riedlinger:2002:HBL

[RG02] Reid Riedlinger and Tom Grutkowski. The high bandwidth, 256KB 2nd level cache on an Itanium microprocessor. In IEEE [IEE02], page ?? ISBN ???? ISSN 0743-1686. LCCN ???? URL `http://cpus.hp.com/technical_references/isscc_2002/isscc_2002_4.shtml`.

Rusu:2004:IPH

[RMC04] Stefan Rusu, Harry Muljono, and Brian Cherkauer. Itanium 2 processor 6M: Higher frequency and larger L3 cache. *IEEE Micro*, 24(2):10–18, March/April 2004. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL `http://csdl.computer.org/comp/mags/mi/2004/02/m2010abs.htm; http://csdl.computer.org/dl/mags/mi/2004/02/m2010.htm; http://csdl.computer.org/dl/mags/mi/2004/02/m2010.pdf`.

Robison:2005:BUD

[Rob05] Arch Robison. N-bit unsigned division via N-bit multiply-add. In IEEE [IEE05], page ?? ISBN ???? LCCN ???? URL `http://arith17.polito.it/final/paper-104.pdf`.

Roelofs:1998:FL

[Roe98] Greg Roelofs. The future of Linux. *Linux Journal*, 54:34–38, October 1998. CODEN LIJOFX. ISSN 1075-3583 (print), 1938-3827 (electronic).

Roothaan:2006:CDC

[Roo06] Clemens C. Roothaan. Compiler design criteria for modulo scheduled Itanium codes. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/; http://www.ice.gelato.org/about/oct06_presentations.php`.

Rusu:2000:FIM

[RS00] S. Rusu and G. Singer. The first IA-64 microprocessor. *IEEE Journal of Solid-State Circuits*, 35(11):1539–1544, ???? 2000. CODEN IJSCBC. ISSN 0018-9200 (print), 1558-173X (electronic).

Rusu:2000:CGD

[RT00] S. Rusu and S. Tam. Clock generation and distribution for the first IA-64 microprocessor. In John H. Wuorinen, editor, *Digest of technical papers: 2000 IEEE International Solid-State*

Circuits Conference, San Francisco Marriott Hotel, 7–9 February 2000, volume 43, pages 176–177. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2000. ISBN 0-7803-5853-8. ISSN 0193-6530. LCCN TK7870 .I58 2000. URL http://ieeexplore.ieee.org/iel5/6780/18154/00839738.pdf. IEEE catalog number 00CH37056.

Sharangpani:2000:IPM

[SA00] Harsh Sharangpani and Ken Arora. Itanium processor microarchitecture. *IEEE Micro*, 20(5):24–43, September/October 2000. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL http://dlib.computer.org/mi/books/mi2000/pdf/m5024.pdf; http://www.computer.org/micro/mi2000/m5024abs.htm.

Samaras:2000:IPC

[Sam00] Bill Samaras. The Itanium processor cartridge. In IEEE [IEE00], page ?? ISBN ???? LCCN ???? URL http://www.hotchips.org/index12.html.

Schlansker:2000:EEP

[SC00] Michael S. Schlansker and B. Ramakrishna Rau Cover. EPIC: Explicitly parallel instruction computing. *Computer*, 33(2):37–45, February 2000. CODEN CPTRB4. ISSN 0018-9162 (print), 1558-0814 (electronic). URL http://dlib.computer.org/co/books/co2000/pdf/r2037.pdf; http://www.computer.org/computer/co2000/r2037abs.htm.

Settle:2003:OII

[SCHL03] Alex Settle, Daniel A. Connors, Gerolf Hoflehner, and Dan Lavery. Optimization for the Intel Itanium architecture register stack. In IEEE [IEE03], pages 115–124. ISBN 0-7695-1913-X. LCCN ???? URL http://rogue.colorado.edu/draco/abstract.php?pub=opt_regstack.pub&paper_dir=papers; http://rogue.colorado.edu/draco/papers/cgo-03-register.pdf; http://rogue.colorado.edu/draco/papers/cgo-03-register.ps. ACM Order No. 530033.

Srinivasan:2006:PMU

[SCL06] R. Srinivasan, J. Cook, and O. Lubeck. Performance modeling using Monte Carlo simulation. *IEEE Computer Architecture Letters*, 5(1):38–41, January 2006. ISSN 1556-6056 (print), 1556-6064 (electronic).

Scott:2001:SFB

[Sco01] D. Scott. Sixty-four bit architecture and the Itanium processor. In Krämer and von Gudenberg [KvG01], pages 20–?? ISBN 0-306-46706-2. LCCN ???? 09.00 EUR / 95.00 USD / 66.50 GBP. URL http://www.wkap.nl/prod/b/0-306-46706-2. Scan 2000, the GAMM–IMACS International

Symposium on Scientific Computing, Computer Arithmetic, and Validated Numerics and Interval 2000, the International Conference on Interval Methods in Science and Engineering were jointly held in Karlsruhe, September 19–22, 2000.

Samaras:2001:IIP

[SCV01a] William A. Samaras, Naveen Cherukuri, and Srinivas Venkataraman. The IA-64 Itanium processor cartridge. *IEEE Micro*, 21(1):82–89, January/February 2001. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL `http://dlib.computer.org/mi/books/mi2001/pdf/m1082.pdf`; `http://www.computer.org/micro/mi2001/m1082abs.htm`.

Samaras:2001:SFI

[SCV01b] William A. Samaras, Naveen Cherukuri, and Srinivas Venkataraman. Special feature: The IA-64 Itanium processor cartridge: For high-performance computing in a multiprocessing system environment, consider this innovative packaging solution. *IEEE Micro*, 21(1):82–89, January/February 2001. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

Snavely:2005:UUU

[SDA05] N. Snavely, S. Debray, and G. R. Andrews. Unpredication, unscheduling, unspeculation: reverse engineering Itanium executables. *IEEE Transactions on Software Engineering*, 31(2):99–115, February 2005. CODEN IESEDJ. ISSN 0098-5589 (print), 1939-3520 (electronic). URL `http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=1401927`.

Shimizu:2001:SMC

[SDC01] Kanna Shimizu, David L. Dill, and Ching-Tsun Chou. A specification methodology by a collection of compact properties as applied to the Intel(R) Itanium^{TM} processor bus protocol. *Lecture Notes in Computer Science*, 2144:340–??, 2001. CODEN LNCSD9. ISSN 0302-9743 (print), 1611-3349 (electronic). URL `http://link.springer-ny.com/link/service/series/0558/bibs/2144/21440340.htm`; `http://link.springer-ny.com/link/service/series/0558/papers/2144/21440340.pdf`.

Sery:2002:AOB

[Ser02] George Sery. Approaching the one billion transistor logic product: Process and design challenges. Technical report, Hewlett–Packard Corporation, Palo Alto, CA, USA, 2002. URL `ftp://download.intel.com/technology/silicon/GeorgeSerySPIE0302.pdf`.

Sharangpani:1999:IIP

[Sha99] Harsh Sharangpani. Intel Itanium processor microarchitecture overview. Technical re-

port, Hewlett–Packard Corporation, Palo Alto, CA, USA, 1999. Presented at Microprocessor Forum, October 6–9, 1999.

Sharangpani:2000:IIP

[Sha00a] Harsh Sharangpani. Intel Itanium processor core. In IEEE [IEE00], page ?? ISBN ???? LCCN ???? URL `http://www.hotchips.org/index12.html`.

Sharangpani:2000:IPC

[Sha00b] Harsh Sharangpani. The Itanium processor core. In IEEE [IEE00], page ?? ISBN ???? LCCN ???? URL `http://www.hotchips.org/index12.html`. Runner-up for best presentation award.

Shacklett:2003:IDC

[Sha03] Mary Shacklett. Itanium in the data center. *Enterprise Networks & Servers*, 9(8):9, 14, August 2003. ISSN 1058-5400.

Shermerhorn:2006:HOL

[She06] Lee Shermerhorn. HP/OSLO Linux scalability tracking and investigations. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_scaltracking_shermerhorn_hp.pdf`.

Sibai:1998:HRN

[Sib98a] Fadi N. Sibai. The hyper-ring network: a cost-efficient topology for scalable multicomputers. In *Proceedings of the 1998 ACM symposium on Applied Computing*. ACM Press, New York, NY, USA, 1998. ISBN 0-89791-969-6. LCCN ???? URL `http://delivery.acm.org/10.1145/340000/330982/p607-sibai.pdf`.

Sibai:1998:PHR

[Sib98b] Fadi N. Sibai. Performance of the hyper-ring multicomputer. In *Proceedings of the 1998 ACM symposium on Applied Computing*, pages 598–606. ACM Press, New York, NY, USA, 1998. ISBN 0-89791-969-6. LCCN ???? URL `http://delivery.acm.org/10.1145/340000/330979/p598-sibai.pdf`.

Swartzlander:2000:SPI

[SJS00] Earl E. Swartzlander, Jr., Graham A. Jullien, and Michael J. Schulte. Subword permutation instructions for two-dimensional multimedia processing in MicroSIMD architectures. In Earl E. Swartzlander, Jr., Graham A. Jullien, and Michael J. Schulte, editors, *IEEE International Conference on Application-Specific Systems, Architectures and Processors: proceedings, July 10–12, 2000; Boston, Massachusetts*, pages 3–14. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2000. ISBN 0-7695-0716-6. LCCN TK7874.6.I572 2000. URL `http://ieeexplore.ieee.org/`

iel5/6949/18693/00862373.pdf.

Sylvester:2001:FPC

[SK01] Dennis Sylvester and Himanshu Kaul. Future performance challenges in nanometer design. In *Proceedings of the 38th Conference on Design Automation Conference*, pages 3–8. ACM Press, New York, NY, USA, 2001. ISBN 1-58113-297-2. LCCN ???? URL http://delivery.acm.org/10.1145/380000/378245/p3-sylvester.pdf.

Settle:2004:CCR

[SLHC04] Alex Settle, Daniel Lavery, Gerolf Hoflehner, and Daniel A. Connors. Compiler controlled register stack management for the Intel Itanium architecture. In ????, editor, *Proceedings of the 3rd Workshop on Explicitly Parallel Instruction Computing Architectures and Compiler Techniques. March, 2004.*, page ?? ????, ????, January 20, 2004. ISBN ???? LCCN ???? URL http://rogue.colorado.edu/draco/abstract.php?pub=epic04-regstack.pub&paper_dir=papers; http://rogue.colorado.edu/draco/papers/epic04-regstack.pdf; http://rogue.colorado.edu/draco/papers/epic04-regstack.ps.

Smith:2000:OCF

[Smi00] Michael D. Smith. Overcoming the challenges to feedback-directed optimization. *ACM SIGPLAN Notices*, 35(7):1–11, July 2000. CODEN SINODQ. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic).

Schlansker:1999:CCB

[SMJ99] Michael Schlansker, Scott Mahlke, and Richard Johnson. Control CPR: A branch height reduction optimization for EPIC architectures. *ACM SIGPLAN Notices*, 34(5):155–168, May 1999. CODEN SINODQ. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic). URL http://www.acm.org:80/pubs/citations/proceedings/pldi/301122/p155-schlansker/. See PLDI'99 proceedings [ACM99].

Sias:2000:AEP

[SmWHA00] John W. Sias, Wen mei W. Hwu, and David I. August. Accurate and efficient predicate analysis with binary decision diagrams. In *Proceedings of the 33rd annual IEEE/ACM international symposium on Microarchitecture December 2000*, pages 112–123. ACM Press, New York, NY, USA, 2000. ISBN 1-58113-196-8. LCCN ???? URL http://delivery.acm.org/10.1145/370000/360141/p112-sias.pdf.

Song:1998:DEI

[Son98] Peter Song. Demystifying EPIC and IA-64. *Microprocessor Report*, 12(1):21–27, Jan-

uary 26, 1998. ISSN 0899-9341. URL http://www.cs.cmu.edu/afs/cs.cmu.edu/academic/class/15740-f00/public/doc/discussions/uniprocessors/ia64/mpr_ia64_demyst_jan98.ps.gz.

Schlansker:1998:EAI

[SR98] Michael S. Schlansker and B. Ramakrishna Rau. EPIC: An architecture for instruction-level parallel processors. Technical Report HPL-99-111, Hewlett–Packard Corporation, Palo Alto, CA, USA, 1998. URL http://www.hpl.hp.com/techreports/.

Singer:2000:FIM

[SR00] G. Singer and S. Rusu. The first IA-64 microprocessor: a design for highly-parallel execution. In John H. Wuorinen, editor, *Digest of technical papers: 2000 IEEE International Solid-State Circuits Conference, San Francisco Marriott Hotel, 7–9 February 2000*, volume 43, pages 422–423. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2000. ISBN 0-7803-5853-8. ISSN 0193-6530. LCCN TK7870 .I58 2000. URL http://ieeexplore.ieee.org/iel5/6780/18154/00839843.pdf. IEEE catalog number 00CH37056.

Stinson:2003:GTG

[SR03] Jason Stinson and Stefan Rusu. A 1.5 GHz third generation Itanium microprocessor. In IEEE, editor, *Digest of technical papers: 2003 IEEE International Solid-State Circuits Conference: Sunday through Thursday, February 9–13, 2003, San Francisco, California*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2003. URL http://sunsite.rediris.es/pub/mirror/intel/Itanium2/download/14_4_slides_r31_nsn.pdf. IEEE Catalog Number 03CH37414.

Schlansker:2000:AHL

[SRM+00] Michael S. Schlansker, B. Ramakrishna Rau, Scott Mahlke, Vinod Kathail, Richard Johnson, Sadun Anik, and Santosh G. Abraham. Achieving high levels of instruction-level parallelism with reduced hardware complexity. Technical Report HPL-96-120, Hewlett–Packard Corporation, Palo Alto, CA, USA, 2000. URL http://www.hpl.hp.com/techreports/.

Seznec:2003:HUL

[SS03] André Seznec and Nicolas Sendrier. HAVEGE: A user-level software heuristic for generating empirically strong random numbers. *ACM Transactions on Modeling and Computer Simulation*, 13(4):334–346, October 2003. CODEN ATMCEZ. ISSN 1049-3301 (print), 1558-1195 (electronic).

Shibata:2001:SIL

[SSN+01] T. Shibata, S. Sakon, J. No-

mura, et al. Software for IA-64 Linux on Express5800/1000 Series. *NEC Technical Journal = NEC giho*, 54(10):52–55, 2001. CODEN NECGEZ. ISSN 0285-4139.

Story:1999:NAI

[ST99] S. Story and P. T. P. Tang. New algorithms for improved transcendental functions on IA-64. In Koren and Kornerup [KK99], pages 4–11. ISBN 0-7803-5609-8, 0-7695-0116-8, 0-7695-0118-4. ISSN 1063-6889. LCCN QA76.6 .S887 1999. URL `http://euler.ecs.umass.edu/paper/final/paper-118.pdf`; `http://euler.ecs.umass.edu/paper/final/paper-118.ps`. IEEE Computer Society Order Number PR00116. IEEE Order Plan Catalog Number 99CB36336.

Stoughton:2002:DPA

[Sto02] Nick Stoughton. Developing portable applications. In USENIX [USE02], page 355. ISBN 1-880446-00-6. LCCN QA76.8.U65 U84 2002. URL `http://www.usenix.org/publications/library/proceedings/usenix02/tech/techonefile.html`. Unpublished guru session talk, 2002 USENIX Annual Technical Conference, June 10-15, 2002, Monterey Conference Center, Monterey, CA.

Shibuya:2001:ISH

[SUK+01] T. Shibuya, I. Uehara, M. Kimura, et al. Itanium 16way server hardware. *NEC Technical Journal = NEC giho*, 54(10):15–18, 2001. CODEN NECGEZ. ISSN 0285-4139.

Svensson:2002:PAI

[Sve02] Fredrik Svensson. Performance analysis on Intel Itanium. Examensarbete, Civilingenjörsprogrammet, Luleå tekniska universitet, Luleå, Sweden, 2002. URL `http://epubl.luth.se/1402-1617/2002/078`.

Senta:2001:ISS

[SYA+01] T. Senta, M. Yamamori, F. Aono, et al. Itanium 16way server system architecture. *NEC Technical Journal = NEC giho*, 54 (10):25–28, 2001. CODEN NECGEZ. ISSN 0285-4139.

Sias:2004:FTI

[SzUK+04] John W. Sias, Sain zee Ueng, Geoff A. Kent, Ian M. Steiner, Erik M. Nystrom, and Wen mei W. Hwu. Field-testing IMPACT EPIC research results in Itanium 2. *ACM SIGARCH Computer Architecture News*, 32 (2):26, March 2004. CODEN CANED2. ISSN 0163-5964 (print), 1943-5851 (electronic).

Takeda:2006:SMS

[Tak06] Shingo Takeda. A security monitoring system for Grid computing. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_gridsecurity_takeda_osakauniv.pdf`.

Tan:2006:TSC

[Tan06] Kenneth Tan. Technical and scientific computing performance: Today and tomorrow. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/`; `http://www.ice.gelato.org/about/oct06_presentations.php`.

Triebel:2001:PIB

[TBB01] Walter Triebel, Joseph D. Bissell, and Rick Booth. *Programming Itanium-based systems: Developing High Performance Applications for Intel's New Architecture*. Intel Corporation, Santa Clara, CA, USA, 2001. ISBN 0-9702846-2-4. xvi + 360 pp. LCCN ????

Tal:1999:ALP

[TBGOD99] Ady Tal, Vadim Bassin, Shay Gal-On, and Elena Demikhovsky. Assembly language programming tools for the IA-64 architecture. *Intel Technology Journal*, (Q4):10, November 22, 1999. URL `http://developer.intel.com/technology/itj/q41999/articles/art_3.htm`; `http://developer.intel.com/technology/itj/q41999/pdf/assemble.pdf`.

Thakkar:1999:ISS

[TH99] Shreekant (Ticky) Thakkar and Tom Huff. The Internet Streaming SIMD Extensions. *Intel Technology Journal*, (Q2): 8, May 17, 1999. ISSN 1535-766X. URL `http://developer.intel.com/technology/itj/q21999/articles/art_1.htm`; `http://developer.intel.com/technology/itj/q21999/pdf/simd_ext.pdf`.

Thompson:1998:JIP

[Tho98] Carol Thompson. Java on IA-64 — A peek into the future of Java performance on Intel's Merced and beyond. *UNIX Review*, 16 (11):41–48, ???? 1998. CODEN UNRED5. ISSN 0742-3136.

Thomas:2003:IMF

[Tho03] James W. Thomas. Inlining of mathematical functions in HP-UX for Itanium 2. In IEEE [IEE03], pages 135–144. ISBN 0-7695-1913-X. LCCN ???? ACM Order No. 530033.

Tirumalai:1990:PLE

[TLS90] Parthasarathy Tirumalai, Meng Lee, and Michael S. Schlansker. Parallelization of loops with exits on pipelined architectures. Technical Report HPL-90-107, Hewlett–Packard Corporation, Palo Alto, CA, USA, 1990. URL `http://www.hpl.hp.com/techreports/`.

Thomas:2004:LLF

[TOML04] James W. Thomas, Jon P. Okada, Peter Markstein, and Ren-Cang Li. The `libm` library and floating-point arithmetic in HP-UX for Itanium-based systems: Updated for HP-UX 11i v2. Technical report, Hewlett–Packard Corporation,

Palo Alto, CA, USA, December 3, 2004. 26 pp. URL http://h21007.www2.hp.com/dspp/ddl/ddl_Download_File_TRX/1,1249,942,00.pdf.

Tam:2000:CGD

[TRD+00] S. Tam, S. Rusu, U. N. Desai, R. Kim, J. Zhang, and I. Young. Clock generation and distribution for the first IA-64 microprocessor. *IEEE Journal of Solid-State Circuits*, 35 (11):1545–1552, November 2000. CODEN IJSCBC. ISSN 0018-9200 (print), 1558-173X (electronic).

Triebel:2000:IAS

[Tri00] Walter Triebel. *Itanium architecture for software developers*. Intel Corporation, Santa Clara, CA, USA, 2000. ISBN 0-9702846-4-0. xxxv + 308 pp. LCCN ????

Tsukakoshi:2001:OIT

[Tsu01] M. Tsukakoshi. Outline of Itanium technical server. *NEC Technical Journal = NEC giho*, 54(10):9–10, 2001. CODEN NECGEZ. ISSN 0285-4139.

Tuomi:2002:LDM

[Tuo02] Ilkka Tuomi. The lives and death of Moore's Law. *First Monday*, 7(11):??, 11 4, 2002. URL http://firstmonday.org/htbin/cgiwrap/bin/ojs/index.php/fm/article/view/1000/921; http://firstmonday.org/issues/issue7_11/tuomi/.

Uhlig:1999:SPS

[UFG+99] Richard Uhlig, Roman Fishtein, Oren Gershon, Israel Hirsh, and Hong Wang. SoftSDV: A presilicon software development environment for the IA-64 architecture. *Intel Technology Journal*, (Q4):14, November 22, 1999. URL http://developer.intel.com/technology/itj/q41999/articles/art_2.htm; http://developer.intel.com/technology/itj/q41999/pdf/softsdv.pdf.

Umesato:2001:HTI

[UMT+01] S. Umesato, S. Mano, T. Takagi, et al. Hardware technology for Itanium 16way server. *NEC Technical Journal = NEC giho*, 54(10):19–24, 2001. CODEN NECGEZ. ISSN 0285-4139.

USENIX:2000:PFW

[USE00] USENIX, editor. *Proceedings of the First Workshop on Industrial Experiences with Systems Software (WIESS 2000), October 22, 2000, Paradise Point Resort, San Diego, California, USA*. USENIX, Berkeley, CA, USA, 2000. ISBN 1-880446-15-4. LCCN QA76.76.S95 W67 2000. URL http://www.usenix.org/publications/library/proceedings/osdi2000/wiess2000/.

USENIX:2002:PGT

[USE02] USENIX, editor. *Proceedings of the General Track: 2002 USENIX Annual Technical Conference, June 10–15, 2002, Monterey, California,*

USA. USENIX, Berkeley, CA, USA, 2002. ISBN 1-880446-00-6. LCCN QA76.8.U65 U84 2002. URL `http://www.usenix.org/publications/library/proceedings/usenix02/`.

Umeki:2001:ISH

[USK+01] T. Umeki, O. Suwa, A. Kobayashi, et al. Itanium 4way server hardware. *NEC Technical Journal = NEC giho*, 54(10):37–39, 2001. CODEN NECGEZ. ISSN 0285-4139.

Velev:2001:EUB

[VB01] Miroslav N. Velev and Randal E. Bryant. Effective use of boolean satisfiability procedures in the formal verification of superscalar and VLIW. In *Proceedings of the 38th Conference on Design Automation Conference 2001*, pages 226–231. ACM Press, New York, NY, USA, 2001. ISBN 1-58113-297-2. LCCN ???? URL `http://delivery.acm.org/10.1145/380000/378469/p226-velev.pdf`.

VanZee:2008:SPF

[VBLvdG08] Field G. Van Zee, Paolo Bientinesi, Tze Meng Low, and Robert A. van de Geijn. Scalable parallelization of FLAME code via the workqueuing model. *ACM Transactions on Mathematical Software*, 34(2):10:1–10:29, March 2008. CODEN ACMSCU. ISSN 0098-3500 (print), 1557-7295 (electronic).

Vishkin:1998:EMT

[VDBN98] Uzi Vishkin, Shlomit Dascal, Efraim Berkovich, and Joseph Nuzman. Explicit multithreading (XMT) bridging models for instruction parallelism (extended abstract). In *SPAA '98: 10th Annual ACM Symposium on Parallel Algorithms and Architectures, June 28–July 2, 1998, Puerto Vallarta, Mexico*. ACM Press, New York, NY, USA, 1998. ISBN 0-89791-989-0. LCCN QA76.58 .A26 1998. URL `http://delivery.acm.org/10.1145/280000/277680/p140-vishkin.pdf`. ACM order number 417980.

VanderWiel:1997:WCA

[VL97] Steven P. VanderWiel and David J. Lilja. When caches aren't enough: Data prefetching techniques. *Computer*, 30(7):23–30, July 1997. CODEN CPTRB4. ISSN 0018-9162 (print), 1558-0814 (electronic). URL `http://dlib.computer.org/co/books/co1997/pdf/r7023.pdf`; `http://www.computer.org/computer/co1997/r7023abs.htm`.

Vachharajani:2004:LSE

[VVP+04] Manish Vachharajani, Neil Vachharajani, David A. Penry, Jason A. Blome, and David I. August. The Liberty Simulation Environment, version 1.0. *ACM SIGMETRICS Performance Evaluation Review*, 31(4):19–24, March 2004. CODEN

???? ISSN 0163-5999 (print), 1557-9484 (electronic).

Wells:2002:CCS

[WAB02] S. Wells, F. Anderson, and E. Berta. The core clock system for a next-generation Itanium processor. In IEEE [IEE02], page ?? ISBN ???? ISSN 0743-1686. LCCN ???? URL `http://www.sscs.org/isscc/`.

Waligora:2002:MVI

[Wal02] Tina Waligora. Medizinische 3D Visualisierungsalgorithmen auf Intel Itanium (64 Bit) Prozessoren unter Windows XP 64 Bit. Diplomarbeit, Stralsund Fachhochschule, Stralsund, Germany, 2002. 90 pp.

Warton:1997:PSI

[War97] John Warton. Panel session: If *I* were defining 'Merced'. In IEEE [IEE97], page ?? ISBN ???? LCCN ????

Wang:2004:HTVa

[WCW+04a] Perry H. Wang, Jamison D. Collins, Hong Wang, Dongkeun Kim, Bill Greene, Kai-Ming Chan, Aamir B. Yunus, Terry Sych, Stephen F. Moore, and John P. Shen. Helper threads via virtual multithreading on an experimental Itanium-2 processor-based platform. *ACM SIGARCH Computer Architecture News*, 32(5):144–155, December 2004. CODEN CANED2. ISSN 0163-5964 (print), 1943-5851 (electronic). Co-published in *Operating Systems Review*, (**38**)(4).

Wang:2004:HTVb

[WCW+04b] Perry H. Wang, Jamison D. Collins, Hong Wang, Dongkeun Kim, Bill Greene, Kai-Ming Chan, Aamir B. Yunus, Terry Sych, Stephen F. Moore, and John P. Shen. Helper threads via virtual multithreading on an experimental Itanium-2 processor-based platform. *ACM SIGPLAN Notices*, 39(11):144–155, November 2004. CODEN SINODQ. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic).

Wang:2004:HTVc

[WCW+04c] Perry H. Wang, Jamison D. Collins, Hong Wang, Dongkeun Kim, Bill Greene, Kai-Ming Chan, Aamir B. Yunus, Terry Sych, Stephen F. Moore, and John P. Shen. Helper threads via virtual multithreading on an experimental Itanium-2 processor-based platform. *Operating Systems Review*, 38(5):144–155, December 2004. CODEN OSRED8. ISSN 0163-5980 (print), 1943-586X (electronic).

Wu:2000:CRL

[WfL00] Youfeng Wu and Yong fong Lee. Comprehensive redundant load elimination for the IA-64 architecture. In Carter and Ferrante [CF00], pages 53–69. ISBN 3-540-67858-1. ISSN 0302-9743 (print), 1611-3349 (electronic). LCCN QA76.58 .L36 2000.

Wichmann:2006:ULO

[Wic06] Mats D. Wichmann. An update on LSB and open standards. In Anonymous [Ano06], page ?? ISBN ???? LCCN ???? URL `http://www.ice.gelato.org/oct06/pres_pdf/gelato_ICE06oct_lsb_wichmann_intel.pdf`.

Wirt:1999:CNS

[Wir99] Richard Wirt. The challenges of new software for a new architecture. *Intel Technology Journal*, November 22, 1999. ISSN 1535-766X.

Wolfe:2004:GTC

[Wol04] Alexander Wolfe. Grid tools: Coming to a cluster near you. *ACM Queue: Tomorrow's Computing Today*, 2(4):20–23, June 2004.

Williams:2006:PCP

[WSO+06] Samuel Williams, John Shalf, Leonid Oliker, Shoaib Kamil, Parry Husbands, and Katherine Yelick. The potential of the cell processor for scientific computing. In ACM [ACM06], pages 9–20. ISBN 1-59593-302-6. LCCN ???? ACM order number 104060.

Weiss:2002:CSB

[WWC02] Don Weiss, John J. Wuu, and Victor Chin. The on-chip 3MB subarray based 3rd level cache on an Itanium microprocessor. In IEEE [IEE02], page ?? ISBN ???? ISSN 0743-1686. LCCN ???? URL `http://cpus.hp.com/technical_references/isscc_2002/isscc_2002_5.shtml`.

Worley:2000:AFP

[WWCW00] John Worley, Bill Worley, Tom Christian, and Christopher Worley. AES finalists on PA-RISC and IA-64: Implementations & performance. In NIST [NIS00], pages 57–74. ISBN ???? LCCN ???? URL `http://csrc.nist.gov/encryption/aes/round2/conf3/aes3conf.htm`; `http://csrc.nist.gov/encryption/aes/round2/conf3/papers/AES3Proceedings-1.pdf`; `http://csrc.nist.gov/encryption/aes/round2/conf3/papers/AES3Proceedings-2.pdf`; `http://csrc.nist.gov/encryption/aes/round2/conf3/papers/AES3Proceedings-3.pdf`; `http://csrc.nist.gov/encryption/aes/round2/conf3/papers/AES3Proceedings.pdf`.

Wang:2001:RRS

[WWK+01] P. H. Wang, Hong Wang, R. M. Kling, K. Ramakrishnan, and J. P. Shen. Register renaming and scheduling for dynamic execution of predicated code. In IEEE, editor, *HPCA: the seventh International Symposium on High-Performance Computer Architecture: proceedings, 19–24 January 2001, Monterrey, Nuevo Leon, Mexico*, pages 15–25. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910,

USA, 2001. ISBN 0-7695-1019-1. LCCN QA76.9.A73 I566 2001.

Wang:2008:OSA

[WYX+08] Li Wang, Xuejun Yang, Jingling Xue, Yu Deng, Xiaobo Yan, Tao Tang, and Quan Hoang Nguyen. Optimizing scientific application loops on stream processors. *ACM SIGPLAN Notices*, 43(7):161–170, July 2008. CODEN SINODQ. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic).

Yi:2000:TLR

[YAK00] Qing Yi, Vikram Adve, and Ken Kennedy. Transforming loops to recursion for multi-level memory hierarchies. *ACM SIGPLAN Notices*, 35(5):169–181, May 2000. CODEN SINODQ. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic). URL `http://www.acm.org/pubs/articles/proceedings/pldi/349299/p169-yi/p169-yi.pdf; http://www.acm.org/pubs/citations/proceedings/pldi/349299/p169-yi/`.

Yeh:1998:RAI

[YP98] Tse-Yu Yeh and Yale N. Patt. Retrospective: alternative implementations of two-level adaptive training branch prediction. In Gurindar Sohi, editor, *25 years of the International Symposia on Computer Architecture (selected papers)*, pages 87–88. ACM Press, New York, NY, USA, 1998. ISBN 1-58113-058-9. LCCN QA76.9.A73 S944 1998. URL `http://delivery.acm.org/10.1145/290000/285964/p87-yeh.pdf`.

Zahir:2000:CCDa

[ZRMH00a] Rumi Zahir, Jonathan Ross, Dale Morris, and Drew Hess. OS and compiler considerations in the design of the IA-64 architecture. *ACM SIGARCH Computer Architecture News*, 28(5): 212–221, December 2000. CODEN CANED2. ISSN 0163-5964 (print), 1943-5851 (electronic). Co-published in *Operating Systems Review*, (**34**)(5).

Zahir:2000:CCDb

[ZRMh00b] Rumi Zahir, Jonathan Ross, Dale Morris, and Drew hess. OS and compiler considerations in the design of the IA-64 architecture. *ACM SIGPLAN Notices*, 35(11):212–221, November 2000. CODEN SINODQ. ISBN 1-58113-317-0. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic).

Zahir:2000:SHIa

[ZRMH00c] Rumi Zahir, Jonathan Ross, Dale Morris, and Drew Hess. Support for high ILP processors — OS and compiler considerations in the design of the IA-64 architecture. *Operating Systems Review*, 34(5):212–221, ???? 2000. CODEN OSRED8. ISSN 0163-5980 (print), 1943-586X (electronic).

Zahir:2000:SHIb

[ZRMH00d] Rumi Zahir, Jonathan Ross, Dale Morris, and Drew Hess. Support for high ILP processors — OS and compiler considerations in the design of the IA-64 architecture. *ACM SIGARCH Computer Architecture News*, 28 (5):212–221, ???? 2000. CODEN CANED2. ISSN 0163-5964 (print), 1943-5851 (electronic).

Zheng:2000:PRI

[ZT00] Cindy Zheng and Carol Thompson. PA-RISC to IA-64: Transparent execution, no recompilation. *Computer*, 33(3):47–52, March 2000. CODEN CPTRB4. ISSN 0018-9162 (print), 1558-0814 (electronic). URL `http://dlib.computer.org/co/books/co2000/pdf/r3047.pdf`; `http://www.computer.org/computer/co2000/r3047abs.htm`.

Zhang:1997:SSA

[ZWG+97] Xiaolan Zhang, Zheng Wang, Nicholas Gloy, J. Bradley Chen, and Michael D. Smith. System support for automatic profiling and optimization. In *Proceedings of the sixteenth ACM symposium on Operating systems principles*. ACM Press, New York, NY, USA, 1997. ISSN 0163-5980 (print), 1943-586X (electronic). URL `http://delivery.acm.org/10.1145/270000/266640/p15-zhang.pdf`.